ISSCC 2012: Overview

A. Mekkaoui

Intro

Use plenary videos at
http://swankav.mediasite.com/mediasite/Catalog/Full/ee0791d3-f75f-4979-a5a0-15deab761291/?state=dqEfeBitG8WInyWOInUl

Link to plenary session videos available. If interested send me an email (amekkaoui@lbl.gov)
CD of the digest of papers is also available.


Attended session (handout available)


Interesting session (presentations listed below)


Interesting paper

"Interesting": very subjective, not necessarily in the technical sense

Sunday, February 19th

ISSCC 2012 Tutorials

T1:
RF Mixers: Analysis and Design Trade-offs
Instructor:
Hooman Darabi

T2:
Flash-Memory Based Circuit, System, and Platform Design
Instructor:
Mark Bauer

T3:
Mobile GHz Processor Design Techniques
Instructor:
Byeong-Gyu Nam

T4:
Wideband Delta-Sigma Modulators
Instructor:
Lucien Breems

T5:
Jitter: Basic and Advanced Concepts, Statistics, and Applications
Instructor:
Nicola Da Dalt

T6:
Power Management Using Integrated Voltage Regulators
Instructor:
Tanay Karnik

T7:
Digital Calibration for RF Transceivers
Instructor:
Albert Jerng

T8:
Managing Offset and Flicker Noise
Instructor:
Axel Thomsen

T9:
Getting In Touch with MEMS: The Electromechanical Interface
Instructor:
Aaron Partridge

ISSCC 2012 Forums

F1:
Beamforming Techniques and RF Transceiver Design

8:00 AM

F2:
Robust VLSI Circuit Design and Systems for Sustainable Society
8:00 AM

ISSCC 2012 Evening Sessions

ES1: Student Research Preview (SRP)

7:30 PM

ES2: What's Next in Robots? ~ Sensing, Processing, Networking Toward Human Brain and Body
8:00 PM

Conference Registration
6:30 AM
to
8:00 PM

T1: RF Mixers: Analysis and Design Trade-offs

Mixers are essential building blocks of every RF transceiver, often compromising the noise and linearity performance of the entire receive or transmit chain. Specifically, the switching action involved in mixing typically dictates the choice of the radio architecture and proper frequency planning to avoid the receiver desensitization. In this tutorial various mixer architectures such as passive and active, current-mode and voltage-mode, and their properties are analyzed and discussed. Of special importance is the noise response of mixers, which is not very well understood due to the nonlinear and time varying nature of the block, and the fact that conventional linear noise analysis applicable to amplifiers often does not hold. We will focus on intuitive and qualitative ways of analyzing the noise of both passive and active mixers as well.

Instructor: Hooman Darabi

Hooman Darabi received the BS and MS degrees both in Electrical Engineering from Sharif University of Technology, Tehran, Iran, in 1994, and 1996, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1999. He is currently a Sr. Technical Director and a Fellow with Broadcom Corporation, Irvine, CA, as a part of the mobile and wireless group. His interests include analog and RF IC design for wireless communications. Dr. Darabi holds over 170 issued or pending patents with Broadcom, and has published over 50 peer-reviewed journal and conference papers.

T2: Flash-Memory Based Circuit, System, and Platform Design

Applications using flash memory are rapidly increasing in number. Different applications of flash memory demand various Circuit, System, Software and Platform Co-Design to optimize usage. Even for a given application these trade-offs should be considered. Unlike tutorials on flash memory in the past that mostly focus on circuit design, this tutorial will consider System, Software, and Platform Design from the application perspective. The tutorial will also be of interest to the broader audience with interests beyond memory field.

Instructor: Mark Bauer

Mark Bauer is a Fellow at Micron working in the NAND Solutions Group where he is responsible for the vertical integration of Non Volatile Memory and memory systems. He joined Micron in 2010 as part of the Numonyx aqusition. Prior to Micron he spent three years at Numonyx on advanced Phase Change Memory designs in technology. From 1985 to 2008 he worked at Intel developing EPROM, NOR Flash, NAND Flash and Phase Change Memory designs. He holds more than 30 US Patents, has published numerous technical papers in the field of Non Volitile Memory, has been an invited speaker at technical conferences, served on the ISSCC Memory Technical Program Committee for 11 years and is currently on the VLSI Symposium Technical Program Committee. He recieved the BSEE from the University of California in 1985.

T3: Mobile GHz Processor Design Techniques

Mobile computing devices such as smart-phones and smart-pads open up new challenges in mobile processor designs in terms of their speed and power targets. Mobile processors are getting more powerful in order to run increasingly complex software. Therefore, the design of high-speed low-power mobile processors is becoming the major challenge. In this tutorial, design techniques for high-speed mobile CPU and GPU are discussed at several design levels. The talk will go through the architecture, circuit, device level optimization and also consider chip-wise power management techniques. Special considerations for cost-effective micro-architectures, high-speed logic, low-power arithmetic, and DVFS will be highlighted.

Instructor: Byeong-Gyu Nam

Byeong-Gyu Nam received his Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007. His Ph.D. work focused on low-power GPU design for mobile devices. From 2007 to 2010, he was with Samsung Electronics, Giheung, Korea, where he worked on the world's first low-power 1-GHz ARM microprocessor design. Dr. Nam is currently with Chungnam National University, Daejeon, Korea, as an assistant professor. His current interests include mobile GPU, embedded CPU, low-power SoC, and their associated SW platforms. He is serving as a program committee member of the IEEE ISSCC, A-SSCC, COOL Chips, and VLSI-DAT.

T4: Wideband Delta-Sigma Modulators

The application space of delta-sigma analog-to-digital converters has been greatly extended during the last few decades with applications ranging from traditional applications such as audio and hearing aids that require only a few (tens of) kHz bandwidth to a multitude of cellular standards that need up to 40MHz bandwidth. To enable this bandwidth range of four orders of magnitude, new innovative wideband delta-sigma architectures and circuits have been developed that operate at GHz rate sampling frequencies. This tutorial gives an introduction to the system design and implementation of wideband delta-sigma modulators. A review of wideband delta-sigma architectures, loop stability, filter implementations and circuit designs is presented. Some case studies illustrate wideband delta-sigma modulators that have bandwidths in the range from several tens of MHz to beyond 100MHz.

Instructor: Lucien Breems

Lucien Breems received the M.Sc. degree and the Ph.D. degree in Electrical Engineering from the Delft University of Technology, The Netherlands, in 1996 and 2001, respectively. From 2000 to 2007 he was with Philips Research, Eindhoven the Netherlands and in 2007 he joined NXP Semiconductors where he currently leads a team working on delta-sigma A/D converters. Since 2008, he has been a lecturer at the Delft University of Technology on the topic of delta-sigma modulation and since 2011 he is a part-time Professor at the Eindhoven University of Technology. His research interests are in the field of mixed-signal circuit design. In 2001, he received the ISSCC "Van Vessem Outstanding Paper Award".

T5: Jitter: Basic and Advanced Concepts, Statistics, and Applications

Jitter and phase noise are key factors that deeply impact the performance of circuits in modern communication applications. Within the industry, many types of jitter must be and are considered, including cycle-to-cycle, accumulated, deterministic, random, total, absolute, integrated, TIE, and more. Understanding the implications of each of these jitter types demands clear jitter term definitions as well as a common understanding of their practical meaning. In response to this need, this tutorial will presents basic and advanced concepts of jitter. The first part of the tutorial will focus on jitter definitions, statistics, and the relationship of jitter to phase noise. The second part of the tutorial will explore the impact of jitter on a variety of applications, drawing on examples from wireline as well as other technical areas. The overall goal of the tutorial is to provide a solid understanding of what jitter is, how to correctly specify it, and to enhance understanding of jitter specifications for different applications.

Instructor: Nicola Da Dalt
Nicola Da Dalt received the Master degree from University of Padova, Italy, in 1994 and the PhD degree from RWTH Aachen, Germany, in 2007, both in Electronic Engineering. From 1996 to 1998 he was with Telecom Italia, Italy, as concept engineer for architectures and synchronization of data transmission networks and satellite communications. Since 1998 he has been with Infineon Technologies, Austria, as an IC design and concept engineer for clock systems in applications ranging from wireline, to memory and wireless. Since March 2005 he leads the Clocking and Interface Systems group. He received the 2010 IEEE Guillemin-Cauer Best Paper Award. He holds four granted patents and is the author of several publications in conferences and journals.

T6: Power Management Using Integrated Voltage Regulators

Aggressive technology scaling has enabled very high levels of transistor integration. Managing total power consumption has emerged as the most challenging task in today's highly complex microprocessor systems. In this tutorial, we will review power management techniques implemented in recent designs. Independent per-core dynamic voltage scaling is proven to be an effective way to minimize power consumption. Due to the size and routing planes, the number of independent platform rails is limited to a very small number. Near-load voltage regulators provide a practical solution. This tutorial includes a survey of recent innovations in near-load voltage regulators.

Instructor: Tanay Karnik
Tanay Karnik is Principal Engineer and Program Director in Intel Lab's Academic Research Office. He received his Ph.D. in Computer Engineering from University of Illinois at Urbana-Champaign in 1995. His research interests are in the areas of variation tolerance, power delivery, soft errors and physical design. He has published 50 technical papers, has 44 issued and 33 pending patents. He received an Intel Achievement Award for the pioneering work on integrated power delivery. Tanay was the General Chair of ASQED'10, ISQED'09, ISQED'08 and ICICDT'08. Tanay is IEEE Senior Member, Associate Editor for TVLSI and Guest Editor for JSSC.

T7: Digital Calibration for RF Transceivers

Designing high-precision RF transceivers in deep submicron technologies is increasingly challenging due to reduced supply headroom, non-linearities of transistors, and large process parameter spread. By taking advantage of the cheaper and faster digital computing power, digital calibration is becoming an increasingly common practice to overcome such challenges and enhance transceiver performance. Calibration techniques covered include I/Q mismatch calibration, DC offset and LO leakage removal, closed-loop power control and envelope tracking, analog filter response calibration, digital pre-distortion for PAs, and antenna tuning. The tutorial will also cover DSP methods and algorithms and provide specific examples of digitally calibrated transceivers.

Instructor: Albert Jerng
Albert Jerng received his BSEE, MSEE from Stanford University, and his PhD EE from MIT in 1994, 1996, and 2006, respectively. While at MIT, he conducted research on CMOS VCO design and digital TX architectures for Gb/s OFDM systems. Since 2007, he has been with Ralink Technologies as Sr. Director for Advanced Circuits and Systems working on Bluetooth and WiFi products, and is now employed as Deputy Director at Mediatek, responsible for the WiFi RF transceiver division, after their merger with Ralink. He is also serving as General Chair for the IEEE RFIC Symposium in 2012.

T8: Managing Offset and Flicker Noise

A large number of circuits require DC accuracy and low noise at low frequencies. Sensor interfaces are a good example, but comparators, ADC's, and many other blocks need it too. This tutorial will provide a review of techniques to achieve low offset and flicker noise.
Techniques such as chopper stabilization, correlated double sampling, autozero, digital startup calibration, and digital background calibration will be reviewed. Implementation examples will be shown and noise and aliasing and other artifacts will be analyzed. Techniques to master these artifacts will be discussed. The ideas will then be taken into the mixed signal domain.

Instructor: Axel Thomsen
Axel Thomsen received his PhD from the Georgia Institute of Technology in 1992. He has held positions at the University of Alabama in Huntsville, University of Texas, and Cirrus Logic. Currently he is a Distinguished Engineer at Silicon Laboratories in Austin, TX. He has worked on chips for industrial measurement, timing, isolation and power applications. He has a strong interest in precision measurement. Currently he is working in the Embedded Mixed Signal Division on data converters and amplifiers. He holds more than 40 patents.

T9: Getting In Touch with MEMS: The Electromechanical Interface

MEMS systems include mechanical structures and electronic sense and drive circuits. Between these is an electromechanical interface, which can be capacitive, piezoresistive, piezoelectric, ferroelectric, electromagnetic, thermal, optical or can take some other form. The selection of this interface is the single most critical decision in the system definition, and it determines the eventual capabilities and limits of the device. The interface fundamentally sets the device's sensitivity, accuracy, drift, ageing, temperature behavior, and environmental capabilities. The interface determines the MEMS production technology and hence the fab selection, the cost structure, and the time to market. This tutorial examines and compares the available options and application drivers. Which interface technologies can be used? Why is one more suitable for a particular application than another? How do they scale? What is on the horizon? The goal is to expand the attendee's potential role from circuit designer to system designer. From "Here is the MEMS device, design the interface circuit." into "Here is the problem, define an optimal solution."

Instructor: Aaron Partridge
Aaron Partridge received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University, Stanford, CA, in 1996, 1999, and 2003, respectively. In 2004 he co-founded SiTime Corp. where he is Chief Science Officer. SiTime is the leading supplier of MEMS oscillators, resonators, and timing devices. From 2001 through 2004 he was Project Manager at Robert Bosch Research and Technology Center, Palo Alto, CA, where he coordinated the MEMS resonator research. He serves on the IEEE International Solid-State Circuits Conference IMMD subcommittee and is the Editorial Chair of the IEEE International Frequency Control Symposium.

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Monday, February 20th						
6:30 AM	Formal Opening of the Conference					**Conference Registration** 6:30 AM to 3:00 PM
8:30 AM	**Session 1**: Plenary Session					
1:30 PM	**Session 2:** High-Bandwidth DRAM & PRAM	**Session 3:** Processors ★	**Session 4:** RF Techniques	**Session 5:** Audio and Power Converters	**Session 6:** Medical, Displays and Imagers ★	
4:00 PM to 7:00 PM	Academic Demonstration Session (ADS)					
5:15 PM	Author Interviews, Book Displays, Social Hour					
ISSCC 2012 Evening Sessions						
8:00 PM	**ES3:** Tecnologies That Could Change the World - You Decide!		**ES4:** Optical PCB Interconnects, Niche or Mainstream?		**EP1:** Is RF Doomed to Digitization? ~ What Shall RF Circuit Designers Do?	

6.1 A Sampling-Based 128×128 Direct Photon-Counting X-Ray Image Sensor with 3 Energy Bins and Spatial Resolution of 60µm/pixel — 1:30 PM

H-S. Kim, KAIST, Daejeon, Korea

In Paper 6.1, KAIST (with Samsung) presents an X-ray image sensor supporting 3-level energy detection for color X-ray imaging in 0.13µm CMOS. 30% smaller pixel pitch per energy-bin and 10× better uniformity without calibration are achieved compared to state-of-the-art technologies. The 8.8×8.8mm² ASIC has a static 4.6µW/pixel power consumption from 3.3V/1.2V supplies.

6.2 A 1.36µW Adaptive CMOS Image Sensor with Reconfigurable Modes of Operation From Available Energy/Illumination for Distributed Wireless Sensor Network — 2:00 PM

J. Choi, University of Michigan, Ann Arbor, MI

In Paper 6.2, the University of Michigan describes a 5×5mm² adaptively reconfigurable image sensor in 0.18µm CMOS using a 2.5T pixel structure that operates at 1.36µW on a supply voltage of 0.8V from harvested energy. In addition, the imager is reconfigurable to operate in high-sensitivity or wide-dynamic-range modes.

6.3 A 0.5V 4.95µW 11.8fps PWM CMOS Imager with 82dB Dynamic Range and 0.055% Fixed-Pattern-Noise — 2:30 PM

M-T. Chung, National Tsing Hua University, Hsinchu, Taiwan

In Paper 6.3, National Tsing Hua University presents a 1.4×1.4mm² PWM image sensor in 0.18µm CMOS with threshold-variation cancelling and a programmable threshold control scheme. A 0.055% pixel FPN and 82dB dynamic range under 0.5V supply voltage operation are achieved.

6.4 A Capacitive Touch Controller Robust to Display Noise for Ultrathin Touch Screen Displays — 2:45 PM

S-H. Byun, Samsung Electronics, Yongin, Korea

In Paper 6.4, Samsung Electronics describes a capacitive touch controller together with an LCD driver integrated in a 24×1.52mm² chip in a 90nm triple-well LDI process, achieving 35dB SNR without software filtering in an LCD on-cell touch screen by using a differential sensing scheme.

6.5 A 160µA Biopotential Acquisition ASIC with Fully Integrated IA and Motion-Artifact Suppression — 3:15 PM

N. van Helleputte, imec, Heverlee, Belgium

In Paper 6.5, imec (with Samsung Advanced Institute of Technology, and KU Leuven) discusses a 3-channel 160µA biopotential acquisition ASIC in 0.18µm CMOS with 200mHz HPF. The chip is capable of rail-to-rail DC offset rejection for suppressing motion artifacts, while achieving 120dB CMRR, 1GΩ input impedance, and 1.3µV_{rms} input-referred noise at 100Hz bandwidth. The 8×5mm² ASIC consumes 192µW from a 1.2V supply.

6.6 CMOS Capacitive Biosensor with Enhanced Sensitivity for Label-Free DNA Detection — 3:45 PM

K-H. Lee, KAIST, Daejeon, Korea

In Paper 6.6, KAIST describes an integrated capacitance-based biosensor with 57.8dB sensitivity and 94.6% detection dynamic range realized in 0.35µm CMOS for label-free detection of oligonucleotides. The 4×5mm² ASIC consumes 2.34mW from a 3.3V supply.

6.7 A 100Mphoton/s Time-Resolved Mini-Silicon Photomultiplier with On-Chip Fluorescence Lifetime Estimation in 0.13µm CMOS Imaging Technology — 4:00 PM

D. Tyndall, University of Edinburgh, Edinburgh, United Kingdom

In Paper 6.7, the University of Edinburgh (with STMicroelectronics, University of Sussex, and Dialog Semiconductor) presents a 1.7×1.3mm² time-resolved single-photon sensor SoC in 0.13µm CMOS with 100Mphoton/s throughput, 22.5µm pitch, 10% fill factor, and 52ps time-resolution for on-chip fluorescence lifetime estimation.

6.8 A Wireless Magnetoresistive Sensing System for an Intra-Oral Tongue-Computer Interface — 4:15 PM

H. Park, Georgia Institute of Technology, Atlanta, GA

In Paper 6.8, Georgia Institute of Technology (with Laval University) highlights a 12-channel dual-band wireless magnetoresistive sensing system in 0.5µm CMOS for an intraoral tongue-computer interface, which can measure the 3D magnetic field within the oral space and convert it to a set of user-defined commands for environmental control. The 3.8×3.7mm² ASIC consumes 700µW from a 1.8V supply, in addition to the 2.6mW consumed by the accompanying MSP430 microcontroller, for a total system power of 3.3mW.

6.9 A CMOS 10kpixel Baseline-Free Magnetic Bead Detector with Column-Parallel Readout for Miniaturized Immunoassays — 4:45 PM

S. Gambini, University of California at Berkeley, Berkeley, CA

In Paper 6.9 the University of California at Berkeley presents a 10kpixel baseline-free magnetic-bead detector implemented in 0.35µm CMOS with column-parallel readout for miniaturized immunoassays, which reduces the array scan time to 8s and achieves 9nT Allan Deviation, enabling detection of sub-1µm particles. The 5.1×3.5mm² ASIC consumes 330mW.

3.1 A 22nm IA Multi-CPU and GPU System-on-Chip — 1:30 PM

S. Siers, Intel, Folsom, CA

In Paper 3.1, Intel unveils the industry's first 22nm 3D transistors in a next-generation processor containing four IA-32 cores, GPU, memory and PCIe controllers.

3.2 A 32-Core RISC Microprocessor with Network Accelerators, Power Management and Testability Features — 2:00 PM

B. Miller, Cavium, Marlboro, MA

In Paper 3.2, Cavium presents its third-generation 65nm MIPS64 processor, which integrates 32 cores with 4MB L2 cache, hardware accelerators and a DDR3 memory controller, while operating at 1.6GHz with a TDP of 40W to 65W.

3.3 The Next-Generation 64b SPARC Core in a T4 SoC Processor — 2:30 PM

J. Shin, Oracle, Santa Clara, CA

In Paper 3.3, Oracle shows its next-generation 40nm T4 processor. The T4 features eight 8-threaded, out-of-order SPARC cores, a 4MB L3 cache, a crossbar and SoC components on a 403mm² die. The chip delivers up to 5× single-thread performance improvement over its predecessor, within the same power envelope.

3.4 32nm x86 OS-Compliant PC On-Chip with Dual-Core Atom® Processor and RF WiFi Transceiver — 3:15 PM

H. Lakdawala, Intel, Hillsboro, OR

In Paper 3.4, Intel introduces an x86-standard OS-compliant SoC with a dual-core 1.6GHz Atom® processor supporting a custom interconnect fabric, integrated voltage regulators, clock generator with SSC, PMU and a fully integrated RF WiFi transceiver. The chip is implemented in a 32nm high-k/metal-gate CMOS process.

3.5 An 800MHz 320mW 16-Core Processor with Message-Passing and Shared-Memory Inter-Core Communication Mechanisms — 3:45 PM

R. Xiao, Fudan University, Shanghai, China

In Paper 3.5, Fudan University discloses a 16-core processor design featuring both message passing and shared-memory inter-core communication mechanisms implemented in 65nm CMOS occupying 9.1mm², and operating at 800MHz, consuming 320mW at 1.3V.

3.6 A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS — 4:15 PM

S. Jain, Intel, Bangalore, India

In Paper 3.6, Intel's 32nm IA-32 core demonstrates ultra-low voltage operation and a wide supply range of 280mV to 1.2V. The chip occupies 2mm², and consumes 2mW at 0.28V operating at 3MHz, to 737mW at 1.2V operating at 915MHz, with a 4.7× improvement in energy efficiency.

3.7 Resonant Clock Design for a Power-Efficient High-Volume x86-64 Microprocessor — 4:45 PM

V. Sathe, AMD, Fort Collins, CO

In Paper 3.7, AMD (with Cyclos Semiconductor and the University of Michigan) shows a resonant clock network with integrated inductors implemented in AMD's 32nm x86-64 processor resulting in a reduction of 24% in clock power and 5-to-10% in total chip power at frequencies above 3GHz.

3.8 A Reconfigurable Distributed All-Digital Clock Generator Core with SSC and Skew Correction in 22nm High-k Tri-Gate LP CMOS — 5:00 PM

Y. Li, Intel, Hillsboro, OR

In Paper 3.8, Intel introduces a reconfigurable SoC clock-generation core to enable digital SSC and clock-skew correction based on an all-digital synthesizable PLL. The design is implemented in a 22nm high-k metal tri-gate process, consuming 3mW at 1V, operating at 3.2GHz, in the low-power mode.

Tuesday, February 21st

ISSCC 2012 Paper Sessions

8:30 AM	**Session 7:** Multi Gb/s Receiver and Parallel I/O Techniques	**Session 8:** Delta-Sigma Converters	**Session 9:** Wireless Transceiver Techniques	**Session 10:** High-Performance Digital ★	**Session 11:** Sensors & MEMS		**Conference Registration** 8:00 AM to 3:00 PM
1:30 PM	**Session 12:** Multimedia & Communications SoCs	**Session 13:** High-Performance Embedded SRAM	**Session 14:** Digital Clocking & PLLs	**Session 15:** mm-Wave & THz Techniques ★	**Session 16:** Switching Power Control Techniques ★	**Session 17:** Diagnostics & Therapeutic Technologies for Health ★	
4:00 PM to 7:00 PM	Industry Demonstration Session (IDS)						
5:15 PM	Author Interviews, Book Displays, Social Hour						

ISSCC 2012 Evening Sessions

8:00 PM	**ES5:** Vision for Future Television	**EP2:** Little-Known Features of Well-Known Creatures ★	**EP3:** What is the Next RF Frontier?

15.1 A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications 1:30 PM

H. Sherry, STMicroelectronics, Crolles, France; University of Wuppertal, Wuppertal, Germany; IEMN / ISEN, Lille, France

In Paper 15.1, STMicroelectronics (with the University of Wuppertal and IEMN/ISEN) presents a 1kpixel silicon-lens integrated camera for active THz applications in 65nm CMOS. Each pixel includes a ring antenna, a resistive mixer, row/col select and an integrate-and-dump circuit.

15.2 280GHz and 860GHz Image Sensors Using Schottky-Barrier Diodes in 0.13µm Digital CMOS 2:00 PM

R. Han, University of Florida, Gainesville, FL; Cornell University, Ithaca, NY

In Paper 15.2, the University of Florida (with Cornell University and the University of Texas at Dallas) presents two terahertz imagers at 280 and 860GHz using Schottky diodes in standard 0.13µm CMOS. The first is a lens-less 16-pixel imager and the second one is a single-pixel detector.

15.3 A 0.28THz 4×4 Power-Generation and Beam-Steering Array 2:30 PM

K. Sengupta, California Institute of Technology, Pasadena, CA

In Paper 15.3, Caltech presents a scalable transmitter architecture for power generation and beamforming at 280GHz in 45nm SOI CMOS. The two-dimensional 4x4 array radiates with an EIRP of +9.4dBm and beam-steers in 2D over 80° in azimuth and elevation.

15.4 A 283-to-296GHz VCO with 0.76mW Peak Output Power in 65nm CMOS 2:45 PM

Y. M. Tousi, Cornell University, Ithaca, NY

In Paper 15.4, Cornell presents a terahertz varactor-less VCO inspired by the theory of coupled-mode oscillators. Two VCOs are implemented at 283 to 296GHz and 318 to 326GHz with peak output powers of 0.76mW and 0.46mW both in a 65nm bulk CMOS.

15.5 A 1V 19.3dBm 79GHz Power Amplifier in 65nm CMOS — 3:15 PM

K-Y. Wang, National Taiwan University, Taipei, Taiwan

In Paper 15.5, National Taiwan University presents a 1V 79GHz power amplifier with 8-path power-combining technique in 65nm CMOS. The power amplifier achieves saturated power of 19.3dBm and PAE of 19.2% for an area of only 0.855mm².

15.6 A 9% Power Efficiency 121-to-137GHz Phase-Controlled Push-Push Frequency Quadrupler in 0.13µm SiGe BiCMOS — 3:30 PM

Y. Wang, Nanyang Technological University, Singapore; Institute of Microelectronics, Singapore

In Paper 15.6, Nanyang Technological University (with the Institute of Microelectronics and MicroArray Technologies) presents an efficient mm-Wave frequency quadrupler at 121 to 137GHz in 0.13µm SiGe BiCMOS. The generated output power is -2.4dBm with core efficiency of 9%, drawing 1.6mA from a 1.6V supply.

15.7 A 144GHz 0.76cm-Resolution Sub-Carrier SAR Phase Radar for 3D Imaging in 65nm CMOS — 3:45 PM

A. Tang, University of California, Los Angeles, Los Angeles, CA

In Paper 15.7, UCLA (with the University of Florida, HRL and Northrop Grumman Aerospace Systems) presents a 144GHz 3D-imaging phase-based radar that alleviates range ambiguity with ranging measurements at different IF frequencies. The 65nm CMOS chipset achieves measured depth resolution of 0.76cm.

15.8 A 2Gb/s-Throughput CMOS Transceiver Chipset with In-Package Antenna for 60GHz Short-Range Wireless Communication — 4:15 PM

T. Mitomo, Toshiba, Kawasaki, Japan

In Paper 15.8, Toshiba presents a 65nm CMOS transceiver chipset incorporating RF chip with in-package antenna and PHY/MAC chip with fast TX-RX switching to optimize MAC throughput. The transceiver achieves 2.07Gb/s throughput over 3cm distance.

15.9 A Low-Power 57-to-66GHz Transceiver in 40nm LP CMOS with -17dB EVM at 7Gb/s — 4:45 PM

V. Vidojkovic, imec, Heverlee, Belgium

In Paper 15.9, imec (with Vrije Universiteit Brussel and Delft University of Technology) presents a 0.7mm², low-power 60GHz transceiver in 40nm CMOS that achieves 7Gb/s data-rate in all 60GHz band channels using a subharmonic injection-locked VCO with 8GHz locking range.

15.10 A 4-Path 42.8-to-49.5GHz LO Generation with Automatic Phase Tuning for 60GHz Phased-Array Receivers — 5:00 PM

L. Wu, Hong Kong University of Science and Technology, Hong Kong, China

In Paper 15.10, HKUST presents a 65nm CMOS 4-path LO generation scheme for mm-Wave phased arrays consisting of injection-locked phase shifters with on-chip successive-approximation calibration that achieves an rms phase step error of 0.93°.

16.1 Near Independently Regulated 5-Output Single-Inductor DC-DC Buck Converter Delivering 1.2W/mm² in 65 nm CMOS

1:30 PM

H-C. Lin, MediaTek, Hsinchu, Taiwan

Paper 16.1 by MediaTek presents a single-inductor 5-output buck converter with adaptive energy-recovery control technique with 67µV/mA cross-regulation and 1.2W/mm² in 65 nm CMOS.

16.2 A High-Stability Emulated Absolute Current Hysteretic Control Single-Inductor 5-Output Switching DC-DC Converter with Energy Sharing and Balancing

2:00 PM

S-W. Wang, KAIST, Daejeon, Korea

Paper 16.2 by KAIST and JDA presents an efficient AMOLED 5-output SIMO DC-DC, using absolute inductor current emulation and 2 flying switched capacitors to reduce voltage stress while balancing and sharing energy. The chip occupies 4.56mm² in a 0.5µm power BCD process.

16.3 Off-the-Line Primary-Side Regulation LED Lamp Driver with Single-Stage PFC and TRIAC Dimming Using LED Forward Voltage and Duty Variation Tracking Control

2:30 PM

J. Hwang, Anaperior Technology, Seoul, Korea

Paper 16.3 by Anaperior Technology presents a 12W LED lamp driver in a 0.35µm BCD process supporting TRIAC dimming with 0.98 power factor using off-the-line primary-side regulation not requiring an optical isolator.

16.4 A 0.18µm CMOS 91%-Efficiency 0.1-to-2A Scalable Buck-Boost DC-DC Converter for LED Drivers 3:15 PM

P. Malcovati, University of Pavia, Pavia, Italy

Paper 16.4 by University of Pavia together with Mindspeed and University of Milano-Bicocca presents a 0.1-to-2A scalable buck-boost DC-DC for LED Drivers with 91%-efficiency occupying 4.125mm² in 0.18µm CMOS with 5V option.

16.5 A 92% Efficiency Wide-Input Voltage Range Switched-Capacitor DC-DC Converter 3:45 PM

V. Ng, University of California at Berkeley, Berkeley, CA

Paper 16.5 by University of California at Berkeley presents a 7.5-to-13.5V switched capacitor DC-DC converter using feedback and feedforward control to regulate a 1.5V output with 92% efficiency in 11.55mm² of a 0.18µm CMOS process.

16.6 An Optimized Driver for SiC JFET-Based Switches Delivering More Than 99% Efficiency 4:15 PM

K. Norling, Infineon Technologies, Villach, Austria

Paper 16.6 by Infineon Technologies presents a 1400V galvanically isolated SiC JFET gate driver for DC-DC converters achieves 99% efficiency using both 0.6µm BiCMOS and 0.8µm BCD process technologies.

16.7 An Adaptive Reconfigurable Active Voltage Doubler/Rectifier for Extended-Range Inductive Power Transmission 4:45 PM

H-M. Lee, Georgia Institute of Technology, Atlanta, GA

Paper 16.7 by Georgia Institute of Technology presents a 13.56MHz inductively coupled power transmission using an automatically reconfigurable active voltage doubler/rectifier with 77% power conversion efficiency occupies 1mm² in a 0.5µm CMOS process.

16.8 Voltage-Boosting Wireless Power Delivery System with Fast Load Tracker by ΔΣ-Modulated Sub-Harmonic Resonant Switching 5:00 PM

R. Shinoda, Keio University, Yokohama, Japan

Paper 16.8 by Keio University presents a 0.18µm CMOS 13.56MHz sub-harmonic resonant switching wireless power delivery system with suppressed spurious emission up to 0.52W with 50% power conversion efficiency occupying 6.25mm² for each of the transmitter and rectifier chips.

17.1 An 8-Channel Scalable EEG Acquisition SoC with Fully Integrated Patient-Specific Seizure Classification and Recording Processor

1:30 PM

J. Yoo, Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates

Paper 17.1 from Masdar Institute of Science and Technology (with imec, MIT, Massachusetts General Hospital and KAIST), describes an 8-channel scalable EEG acquisition system. The 25mm², 0.18µm CMOS chip integrates an EEG analog front-end with an application-specific seizure-classification processor, resulting in a power consumption as low as 2.03µJ per classification within a 2-second classification window.

17.2 A 259.6µW Nonlinear HRV-EEG Chaos Processor with Body Channel Communication Interface for Mental Health Monitoring

2:00 PM

T. Roh, KAIST, Daejeon, Korea

Paper 17.2 from KAIST, describes an IC for mental-health-status monitoring, which is designed to be integrated into a fabric headband. The 0.13µm CMOS chip integrates a sensor front-end, ADC, custom algorithmic processing and body-channel communication within 11.75mm². Total system power consumption is less than 260µW when acquiring and processing EEG signals for stress analysis.

17.3 A Sub-10nA DC-Balanced Adaptive Stimulator IC with Multimodal Sensor for Compact Electro-Acupuncture System — 2:30 PM

K. Song, KAIST, Daejeon, Korea

Paper 17.3 from KAIST presents an adaptive stimulator IC for a compact electro-acupuncture patch system. The 0.13µm CMOS chip consumes 6.8mW at 1.2V, and supports 32 different drive current levels with high-precision DC balancing (< 10nA).

17.4 A Batteryless 19µW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC — 3:15 PM

F. Zhang, University of Washington, Seattle, WA

Paper 17.4 from the University of Washington (with the University of Virginia) describes a wireless sensor node SoC powered solely from a body-worn thermoelectric generator. Implemented in 0.13µm CMOS, the chip dissipates less than 19µW while performing ECG heart-rate extraction and wireless transmission at 400/433MHz.

17.5 A 1V 5mA Multimode IEEE 802.15.6/Bluetooth Low-Energy WBAN Transceiver for Biotelemetry Applications — 3:45 PM

A. Wong, Toumaz, Abingdon, United Kingdom

Paper 17.5 from Toumaz describes a multi-mode wireless transceiver for wireless body-area networks. The power consumption of the 0.13µm CMOS chip is 5mW for continuous 2.4GHz RX/TX, while satisfying IEEE 802.15.6/Bluetooth-LE PHY requirements.

17.6 A mm-Sized Wirelessly Powered and Remotely Controlled Locomotive Implantable Device — 4:15 PM

A. Yakovlev, Stanford University, Stanford, CA

Paper 17.6 from Stanford presents a mm-sized wireless implantable system capable of controlled motion in fluid, implemented in 65nm CMOS. A 1.86GHz carrier delivers 500µW into the device to power locomotion, propelling the implant at a speed of 0.5cm/s.

17.7 A CMOS Impedance Cytometer for 3D Flowing Single-Cell Real-Time Analysis with ΔΣ Error Correction — 4:45 PM

K-H. Lee, KAIST, Daejeon, Korea

Paper 17.7 from KAIST (with Korea University) describes a system designed to sort and analyze single cells in a microfluidic channel. The 0.13µm 0.38mm² CMOS IC compensates for the differential electrode drift in real-time for a total power consumption of 7.6mW.

10.1 A 280mV-to-1.1V 256b Reconfigurable SIMD Vector Permutation Engine with 2-Dimensional Shuffle in 22nm CMOS

8:30 AM

S. Hsu, Intel, Hillsboro, OR

In Paper 10.1, Intel describes a 0.048mm² 280mV-to-1.1V 256b reconfigurable SIMD vector permutation engine with 2D shuffle in 22nm CMOS. Wide dynamic supply scalability across 280mV (subthreshold) to 1.1V increases the permutation engine's energy-efficiency by 9×.

10.2 A Source-Synchronous 90Gb/s Capacitively Driven Serial On-Chip Link Over 6mm in 65nm CMOS

9:00 AM

S Höppner, Technical University Dresden, Dresden, Germany

In Paper 10.2, Technische Universität Dresden presents a serial on-chip link over 6mm with 43µm bus width in a 65nm LP process, with an energy efficiency of 174fJ/mm at the highest speed of 90Gb/s (10Gb/s/line) and 1.25V V_{DD}. The circuit includes a SerDes transceiver with source-synchronous instantaneously stoppable clocking architecture and data synchronization for globally asynchronous locally synchronous (GALS) systems.

10.3 A 1.45GHz 52-to-162GFLOPS/W Variable-Precision Floating-Point Fused Multiply-Add Unit with Certainty Tracking in 32nm CMOS

9:30 AM

H. Kaul, Intel, Hillsboro, OR

In Paper 10.3, Intel describes a 0.045mm² IEEE single-precision floating-point-fused multiply-add unit fabricated in 32nm CMOS that achieves 52GFLOPS/W at 1.45GHz, 1.05V, 25°C. The device provides up to 4× higher throughput and 3.1× higher energy efficiency at 162GFLOPS/W with single-precision accuracy. Robust near-threshold circuits operating from 300mV to 1.2V enable a peak energy efficiency of 1.2TFLOPS/W.

10.4 A 2.05GVertices/s 151mW Lighting Accelerator for 3D Graphics Vertex and Pixel Shading in 32nm CMOS **9:45 AM**

F. Sheikh, Intel, Hillsboro, OR

In Paper 10.4, Intel fabricates a 0.064mm² single-cycle-throughput lighting accelerator for 3D graphics in a 32nm CMOS process. The design enables 560mV-to-1.2V operation with 2.05Gvertices/s throughput and 0.56% mean error measured at 1.05V, 25°C, and a 47% reduction in critical-path logic stages.

10.5 A 3D System Prototype of an eDRAM Cache Stacked Over Processor-Like Logic Using Through-Silicon Vias **10:15 AM**

M. Wordeman, IBM T. J. Watson, Yorktown Heights, NY

In Paper 10.5, IBM fabricates eDRAM-based L3 cache memory chips in 45nm logic technology stacked on a processor proxy chip and interconnected with 50µm pitch TSVs. The design utilizes a modular cascading multiplexor circuit for inter-layer communication and a stack-wide shorted clock tree for high-frequency synchronous signaling to achieve inter-layer memory accesses up to 2.7GHz.

10.6 3D-MAPS: 3D Massively Parallel Processor with Stacked Memory **10:45 AM**

S-K. Kim, Georgia Institute of Technology, Atlanta, GA

In Paper 10.6, Georgia Tech (with KAIST and Amkor Technology) presents 3D-MAPS, a 3D die-stack many-core processor integrating a logic die with 64 277MHz general-purpose processor cores and a memory die with 256KB of SRAM. This processor at 0.13µm contains 33M transistors, 50K TSVs, and 50K face-to-face pads in a 25mm² footprint and runs at 1.5V consuming up to 6.3W.

10.7 Centip3De: A 3930DMIPS/W Configurable Near-Threshold 3D Stacked System with 64 ARM Cortex-M3 Cores **11:15 AM**

D. Fick, University of Michigan, Ann Arbor, MI

In Paper 10.7, the University of Michigan presents Centip3De – a chip that integrates 64 Cortex-M3 cores in a 3D stacked process and achieves 3930DMIPS/W in 0.13µm LP technology. It exploits near-threshold computing to create configurable compute clusters with 1-to-4 cores operating at 670mV and occupying 63mm².

10.8 K Computer: 8.162 PetaFLOPS Massively Parallel Scalar Supercomputer Built with Over 548k Cores **11:45 AM**

H. Miyazaki, Fujitsu, Kanagawa, Japan

In Paper 10.8, Fujitsu (with RIKEN) describes the K computer system, which integrates over 548k cores using SPARC64 VIIIfx and the Tofu interconnect. It is currently ranked number one in the TOP500 list of supercomputers with a speed of 8.162PFLOPS, 93% efficiency and 9.89MW power consumption.

Creatures

Asad A. Abidi, *University of California, Los Angeles, CA*
Intuition can fail on understanding circuits that are beyond the elementary building blocks discussed in textbooks. We are able to produce complex circuits because they are cascades of these blocks assembled in unilateral signal flows. But this does not describe some of the most interesting and powerful circuits, which are governed by such constraints as modes dictated by symmetry, reciprocity, complex signal paths, and energy conservation. I will bring to light some of these circuits.

A. Paul Brokaw, *Integrated Device Technology, Tucson, AZ*
Digital ICs and the systems that use them grow ever more complex, and I notice that the people who make the ICs like to boast about how many transistors they used to make some useful function. As an Analog circuit designer I get more satisfaction in finding how to use the fewest transistors to obtain some function or level of performance. Years ago, Barrie Gilbert and I were talking about how we enjoyed finding a way to do something new, or improve something old with a handful of transistors. We were commiserating about how we anticipated exhausting the things that could be done with a few transistors at the core of some function. Here we are, more than twenty-five years later, rejoicing that we two, among many others, still find new uses for simple circuits.

Rinaldo Castello, *University of Pavia, Pavia, Italy*
The ultimate performance of a mixed signal SoC is almost always determined by its "simple" analog portion. An intuitive understanding of the intricacy of analog circuits is necessary to maximize their Dynamic Range - the "Holy Grail" of analog design. Nonetheless, the "correct" DR may not be always targeted. For example the frequency interval where noise is important may be different from that for which linearity matters. The characteristics of commonly used analog blocks (especially their frequency dependence) will made intuitively understandable using unconventional techniques. Issues like the ratio between driving and input impedance (current versus voltage mode operation), and between processing and signal bandwidth will be quantified.

Mark Horowitz, *Stanford University, Stanford, CA*
While transistor models are getting even more complex, it is amazing what one can still estimate in your head (with simple aids) using simple models of transistors: from how to size all digital gates, to how input slope affects gate delay, to why precharge gates are faster than CMOS static logic. Using these rules you can easily tell if your synthesis program is doing its job, and what you need to improve your critical paths. More interestingly, this principle can be used to estimate the performance of different logic families to quickly see which might be promising, and which are bunk.

Thomas H. Lee, *Defense Advanced Research Project Agency, Arlington, VA*
Common circuits and devices can sometimes be made to perform unnatural acts, such as getting silicon transistors to emit light (and not just from incandescence from overload). We'll present some of those somewhat in the spirit of a "Circuit Mythbusters."

David Robertson, *Analog Devices, Wilmington, MA*
Most circuit approaches have some "primary benefit" and a series of "side effects". Most of these side-effects are disadvantageous or undesirable, but every once in a while, the side effect may provide some serendipitous benefit: the "bug" may actually be a "feature." One of my favorite examples of this is Barrie Gilbert's Translinear Principle - many designers use a bipolar differential pair as a gain stage, making an assumption of a "linear gm" for a given bias current. In embracing the exponential function of the transistor, Barrie and others unlocked an enormous world of functionality. A more recent example would be the observation that noise in certain parts of an ADC with redundancy can provide "dither" that may actually improve the effective linearity performance. The key to being a "beneficiary" of these side-effects, rather than a victim, is the designer's depth of understanding of how the circuit/architecture really works.

Wednesday, February 22nd

ISSCC 2012 Paper Sessions

8:30 AM	**Session 18:** Innovative Circuits in Emerging Technologies	**Session 19:** 20+Gb/s Wireline Transceivers & Injection-Locked Clocking	**Session 20:** RF Frequency Generation	**Session 21:** Analog Techniques ★	**Session 22:** Image Sensors ★		**Conference Registration** 8:00 AM to 3:00 PM
1:30 PM	**Session 23:** Advances in Heterogeneous Integration	**Session 24:** 10GBASE-T & Optical Fron-tends	**Session 25:** Non-Volatile Memory Solutions	**Session 26:** Short-Range Wireless Transceivers	**Session 27:** Data Converter Techniques ★	**Session 28:** Adaptive & Low-Power Circuits	
5:15 PM	Author Interviews						

21.1 A 0.3-to-1.2GHz Tunable 4th-Order Switched g_m-C Bandpass Filter with >55dB Ultimate Rejection and Out-of-Band IIP3 of +29dBm — 8:30 AM

M. Darvishi, University of Twente, Enschede, The Netherlands

Paper 21.1 by University of Twente presents a 0.3-to-1.2GHz tunable 4th-order BPF that integrates poly-phase g_m-C and N-path techniques to improve the shape and ultimate rejection compared to a simple 4-path filter. The prototype operates from a 1.2V supply and occupies 0.127mm² in a 65nm CMOS process.

21.2 A 0.55V 61dB-SNR 67dB-SFDR 7MHz 4th-Order Butterworth Filter Using Ring-Oscillator-Based Integrators in 90nm CMOS — 9:00 AM

B. Drost, Silicon Laboratories, Corvallis, OR; Oregon State University, Corvallis, OR

Paper 21.2 by Silicon Laboratories and Oregon State University presents a 7MHz bandwidth 4th-order Butterworth filter that achieves 61dB SNR 67dB SFDR and operates from a 0.55V supply. A ring-oscillator-based integrator is used as an alternative to conventional OTA-based integrators. The design occupies 0.29mm² in a 90nm CMOS process.

21.3 A 65nm CMOS 1-to-10GHz Tunable Continuous-Time Lowpass Filter for High-Data-Rate Communications — 9:30 AM

F. Houfaf, STMicroelectronics, Crolles, France; IEMN / ISEN, Lille, France; University of Twente, Enschede, The Netherlands

Paper 21.3 by STMicroelectronics together with IEMN/ISEN and University of Twente presents a GHz range g_m-C low pass filter that occupies 0.01mm² in 65nm CMOS and achieves a tunable cut-off frequency of up to 10GHz with a 1.4V supply, more than 3 times higher than the highest cut-off frequency reported to date.

21.4 A 0.0025mm² Bandgap Voltage Reference for 1.1V Supply in Standard 0.16µm CMOS — 9:45 AM

A-J. Annema, University of Twente, Enschede, The Netherlands

Paper 21.4 by University of Twente and Anagear presents a bandgap voltage reference in 0.16µm CMOS that generates a reference voltage of 0.94V with σ=0.84%. Its small active area of 50×50µm² enables local generation of reference voltages across the chip.

21.5 A 5.58nW 32.768kHz DLL-Assisted XO for Real-Time Clocks in Wireless Sensing Applications **10:15 AM**

D. Yoon, University of Michigan, Ann Arbor, MI

Paper 21.5 by University of Michigan presents a crystal oscillator that consumes 79% less power than the lowest reported at the same oscillation frequency. The chip occupies 0.3mm² in 0.18µm CMOS technology and maintains frequency performance of the crystal over a wide operating range.

21.6 A 0.016mm² 144µW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load with >0.95MHz GBW **10:45 AM**

Z. Yan, University of Macau, Macau, China

Paper 21.6 by University of Macau and Instituto Superior Tecnico presents a 0.016mm² 144µW three-stage amplifier in 0.35µm CMOS combining current-buffer Miller compensation and parasitic-pole cancellation that achieves 4.48× improvement in the FOM compared to previously reported amplifiers.

21.7 A 90V_{pp} 720MHz GBW Linear Power Amplifier for Ultrasound Imaging Transmitters in BCD6-SOI **11:15 AM**

D. Bianchi, University of Pavia, Pavia, Italy

Paper 21.7 by Università degli Studi di Pavia and STMicroelectronics presents the first integrated linear amplifier suited for ultra-sound harmonic imaging systems that achieves the highest gain-bandwidth product at large output voltage swing with a small static dissipation of 37mW. The design occupies 3.2mm² in a BCD6-SOI technology that embeds 5V npn bipolar devices and 0.35µm CMOS with a nominal supply of 3.5V.

21.8 On-Chip Gain Reconfigurable 1.2V 24µW Chopping Instrumentation Amplifier with Automatic Resistor Matching in 0.13µm CMOS **11:30 AM**

F. Michel, KU Leuven, Leuven, Belgium

Paper 21.8 by KU Leuven presents a 1.2V 24µW fully integrated direct-current feedback instrumentation amplifier with rail-to-rail output that is implemented in 0.13µm CMOS. Feedback resistors are integrated on-chip for a small size of 0.465 mm² and low cost.

21.9 A Capacitively Coupled Chopper Instrumentation Amplifier with a ±30V Common-Mode Range, 160dB CMRR and 5µV Offset **11:45 AM**

Q. Fan, Delft University of Technology, Delft, The Netherlands

Paper 21.9 by Delft University of Technology presents a capacitively coupled instrumentation amplifier has ±30V input CM range and achieves 6.5× better NEF, 64× lower power consumption and 17dB higher CMRR compared to previous art. Implemented in a HV CMOS 0.7µm technology, the design operates from a 3V supply.

21.10 A 60V Capacitive-Gain 27nV/√Hz 137dB CMRR PGA with ±10V Inputs **12:00 PM**

C. Birk, Analog Devices, Cork, Ireland

Paper 21.10 by Analog Devices presents a 60V programmable gain amplifier with ±10V differential input range that uses a capacitive gain architecture to achieve high gain and small input-referred noise. This circuit, occupying 3.08mm² in a 0.18µm technology with high-voltage devices, can acquire small voltage signals in the presence of very large common-mode voltages.

22.1 An 83dB-Dynamic-Range Single-Exposure Global-Shutter CMOS Image Sensor with In-Pixel Dual Storage — 8:30 AM

M. Sakakibara, Sony, Atsugi, Japan

In Paper 22.1, Sony (with Sony Semiconductor) describes a single-exposure 5Mpixel, global-shutter CMOS image sensor with an in-pixel storage node. An extended dynamic range of 83dB, a full-well capacity of 67,700e^-, readout noise of 4.8e^-_{rms}, and parasitic light sensitivity (MEM/FD) of less than 100dB are reported.

22.2 A Global-Shutter CMOS Image Sensor with Readout Speed of 1Tpixel/s Burst and 780Mpixel/s Continuous — 9:00 AM

Y. Tochigi, Tohoku University, Sendai, Japan

In Paper 22.2, Tohoku University (with Link Research, and Shimadzu) presents a global-shutter 400(H)×256(V) pixel CMOS image sensor including 128 on-chip memory elements/pixel with a capture speed of 10Mfps in burst operation without cooling, and a readout speed of 7.8kfps in continuous operation.

22.3 A 0.7e^-_{rms}-Temporal-Readout-Noise CMOS Image Sensor for Low-Light-Level Imaging — 9:30 AM

Y. Chen, Delft University of Technology, Delft, The Netherlands

In Paper 22.3, Delft University of Technology (with Teledyne DALSA Semiconductors, CMOSIS NV, and Harvest Imaging) describes a CMOS imager that combines in-pixel buried-channel source followers, column-level amplifiers, and correlated multiple sampling by column-parallel single-slope ADCs, resulting in 0.7e^- temporal readout noise.

22.4 A 256×256 CMOS Image Sensor with ΔΣ-Based Single-Shot Compressed Sensing **10:15 AM**

Y. Oike, Stanford University, Stanford, CA; Sony, Atsugi, Japan

In Paper 22.4, Stanford University (with Sony) highlights a 256×256 CMOS image sensor with column-parallel ΔΣ ADC and built-in single-shot compressed sensing during A/D conversion. Compression ratios of 1/4, 1/8, and 1/16 are achieved at 480, 960 and 1920fps, respectively. Readout noise (351μV$_{rms}$) and power consumption (96.2mW) are unchanged from 120 to 1920fps.

22.5 A 33Mpixel 120fps CMOS Image Sensor Using 12b Column-Parallel Pipelined Cyclic ADCs **10:45 AM**

T. Watabe, NHK Science & Technology Research Laboratories, Tokyo, Japan

In Paper 22.5, NHK Science & Technology Research Laboratories (with Shizuoka University, and Brookman Technology) demonstrate a CMOS image sensor with 12b column-parallel pipelined cyclic ADCs and 96 parallel LVDS output ports, resulting in a total output data rate of 51.2Gb/s for the 33Mpixel large-pixel array operated at 120fps. The sensor read noise is 6.1e$^-$ at 0.96 gain and 3.9e$^-$ at 6.8 gain in the readout chain, at a power consumption of 2.32W and 2.54W, respectively. An input-referred ADC noise of 148.5μV$_{rms}$ is reported.

22.6 A 14b Extended Counting ADC Implemented in a 24MPixel APS-C CMOS Image Sensor **11:00 AM**

J-H. Kim, Samsung Electronics, Yongin, Korea

In Paper 22.6, Samsung Electronics presents a CMOS image sensor employing an extended counting ADC with 14b of resolution and 12.8μs conversion time. A full-frame still-shot mode with 6.5fps, 14b resolution, and 24Mpixel operation, as well as a video mode with 30fps,10b resolution, and 6Mpixel operation are supported. The reported full-frame power consumption is 1.25W, and the read noise is 420μV$_{rms}$.

22.7 A 1.5Mpixel RGBZ CMOS Image Sensor for Simultaneous Color and Range Image Capture **11:15 AM**

W. Kim, Samsung Electronics, Hwasung, Korea

In Paper 22.7, Samsung Electronics (with Samsung Semiconductor) introduces a 1.5Mpixel RGBZ FSI CMOS image sensor with 1920(H)×720(V) 2.25×2.25μm^2 2.5T RGB pixels and 480(H)×360(V) 2.25×9.0μm^2 5T single-tap Z pixels. The Z-pixels are organized in horizontal rows in-between the RGB color pixel rows. A range error of 0.5 to 2.5% from 1 to 7m with a 10ms integration time and modulation frequency of 20MHz is reported.

22.8 A QVGA-Range Image Sensor Based on Buried-Channel Demodulator Pixels in 0.18μm CMOS with Extended Dynamic Range **11:45 AM**

L. Pancheri, Fondazione Bruno Kessler, Trento, Italy

In Paper 22.8, Fondazione Bruno Kessler reports a QVGA CMOS image sensor with buried-channel photo-demodulator pixels for time-of-flight range imaging. The sensor has a pixel pitch of 14μm with a fill-factor of 48%, allowing a maximum frame rate of 70 3D fps. Dynamic range extension using multiple-exposure times is demonstrated.

22.9 A 1920×1080 3.65μm-Pixel 2D/3D Image Sensor with Split and Binning Pixel Structure in 0.11μm Standard CMOS **12:00 PM**

S-J. Kim, Samsung Advanced Institute of Technology, Yongin, Korea

In Paper 22.9, Samsung Advanced Institute of Technology highlights a RGBZ CMOS image sensor based on standard pinned photodiodes binned together in time-of-flight mode, generating both a 1920(H)×1080(V) color image as well as a 480(H)×270(V) range image. The pixel demodulates a 20MHz time-of-flight signal with 52.8% contrast. The range error is smaller than 38mm between 0.75 and 4.0m.

27.1 A 14b 3/6GHz Current-Steering RF DAC in 0.18µm CMOS with 66dB ACLR at 2.9GHz

1:30 PM

G. Engel, Analog Devices, Wilmington, MA

In Paper 27.1, Analog Devices present a 14b 3/6GHz current-steering RF DAC in 0.18µm CMOS. Using different switch-driving modes, several frequency bands are covered. A 66dB ACLR at 2.9GHz is demonstrated.

27.2 Ring Amplifiers for Switched-Capacitor Circuits

2:00 PM

B. Hershberg, Oregon State University, Corvallis, OR

In Paper 27.2, Oregon State University (with Asahi Kasei) introduces a concept for operating switched-capacitor circuits at low power. The concept is demonstrated using a 15b 20MHz pipelined converter designed in 0.18µm CMOS, running at an efficiency of 45fJ/conversion-step.

27.3 A 5.37mW 10b 200MS/s Dual-Path Pipelined ADC

2:30 PM

Y. Chai, National Chiao Tung University, Hsinchu, Taiwan

In Paper 27.3, National Chiao Tung University shows a 10b 200MS/s pipelined converter implemented in 65nm CMOS that consumes 5.37mW. The low power consumption is achieved using a dual-path concept. Two amplifiers per pipelined stage allow individual optimization, resulting in an overall improved power efficiency.

27.4 A 13b 315fs$_{rms}$ 2mW 500MS/s 1MHz Bandwidth Highly Digital Time-to-Digital Converter Using Switched Ring Oscillators **3:15 PM**

A. Elshazly, Oregon State University, Corvallis, OR

In Paper 27.4, Oregon State University demonstrates a 13b 315fs$_{rms}$ time-to-digital converter based on a switched ring oscillator that achieves 1st-order noise shaping. This architecture, implemented in 90nm CMOS, overcomes sensitivity to leakage, which was inherent to previous gated ring oscillator TDC designs.

27.5 A 1.7mW 11b 250MS/s 2× Interleaved Fully Dynamic Pipelined SAR ADC in 40nm Digital CMOS **3:45 PM**

B. Verbruggen, imec, Leuven, Belgium

In Paper 27.5, imec (with Renesas) demonstrates an 11b 250MS/s converter designed in 40nm CMOS, which consumes 1.7mW, yielding an energy efficiency of less than 10fJ/conversion-step. Low-power operation is achieved with a 2× time-interleaved pipelined SAR converter using dynamic residue amplification.

27.6 A 90MS/s 11MHz Bandwidth 62dB SNDR Noise-Shaping SAR ADC **4:15 PM**

J. Fredenburg, University of Michigan, Ann Arbor, MI

In Paper 27.6, the University of Michigan introduces the concept of noise shaping into a SAR converter implemented in 65nm CMOS. This is accomplished with an additional memory capacitor for the conversion residue, which is used during the subsequent conversion cycle. An SNDR of 62dB in 11MHz bandwidth at 4× oversampling is achieved.

27.7 A 70dB DR 10b 0-to-80MS/s Current-Integrating SAR ADC with Adaptive Dynamic Range **4:45 PM**

B. Malki, imec, Leuven, Belgium; Vrije Universiteit Brussel, Brussels, Belgium

In Paper 27.7, imec (with Vrije Universiteit Brussel, and Renesas Electronics) demonstrate a 0-to-80MS/s current-integrating SAR converter in 40nm-LP CMOS. The input information steers a programmable transconductor feeding a charge-domain SAR. Parametric amplification relaxes the comparator requirements. This yields 70dB dynamic range.

27.8 A 7-to-10b 0-to-4MS/s Flexible SAR ADC with 6.5-to-16fJ/conversion-step **5:00 PM**

P. Harpe, Holst Centre / imec, Eindhoven, The Netherlands;
Eindhoven University of Technology, Eindhoven, The Netherlands

In Paper 27.8, Holst Centre/imec (with Eindhoven University of Technology) exploits an additional degree of freedom in combining a reconfigurable capacitor array with a noise-adjustable comparator. Together with an optional redundant mode, this yields a 7-to-10b, 0-to-40MS/s, 6.5-to-16fJ/conversion-step converter in 90nm CMOS.

27.9 A 31.3fJ/conversion-step 70.4dB SNDR 30MS/s 1.2V Two-Step Pipelined ADC in 0.13µm CMOS **5:15 PM**

H-Y. Lee, Oregon State University, Corvallis, OR

In Paper 27.9, Oregon State University (with National Semiconductor) demonstrates a pipelined converter with an energy efficiency of 31.3fJ/conversion-step. This is achieved with a 2-step approach at the residue amplification stage. The ADC is implemented in 0.13µm CMOS and achieves 70.4dB SNDR at 30MS/s.

Thursday, February 23rd

ISSCC 2012 Short Course

8:00 AM	Low-Power Analog Signal Processing 8:00 AM to 4:30 PM				**Conference Registration** 7:00 AM to 1:00 PM Short Course and Forum Attendees **Only**
	Ultra-Low-Power/Ultra-Low-Voltage Analog Circuit Design	Power Limits for Amplifiers and Filters	Energy Limits in Current A/D Converter Architectures	Low-Power and Low-Voltage DC-DC Converter Design	

ISSCC 2012 Forums

8:00 AM	**F3:** 10-40 Gb/s I/O Design for Data Communications 8:00 AM to 5:00 PM	**F4:** Computational Imaging 8:00 AM to 4:30 PM	**F5:** Bioelectronics for Sustainable Healthcare 8:00 AM to 5:00 PM	**F6:** Power/Performance Optimization of Many-Core Processor SoCs 8:00 AM to 4:50 PM	

OUTLINE

Ultra-Low-Power/Ultra-Low-Voltage Analog Circuit Design

The supply voltage of CMOS chips has been scaled down in recent years, today reaching the sub-1V region. Analog circuits unfortunately do not take advantage of this voltage scaling. In fact, almost all analog performance metrics are degraded at lower voltages. We first recall the fundamental limits of the design of low-power analog circuits. We then look at the main challenges when designing analog circuits for ultra-low-voltage (ULV) operation. We take a closer look at the MOS transistor operation with a particular focus on weak inversion. We then review several basic building blocks capable of operating at ULV.

Instructor: Christian Enz is VP heading the Integrated and Wireless Systems Division of the Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, Switzerland. He is also Professor at the Swiss Federal Institute of Technology, Lausanne (EPFL), where he is lecturing and supervising students in the field of analog and RF IC design. He received the PhD from the EPFL in 1989. His technical interests and expertise are in the field of ultralow-power analog and RF IC design, wireless sensor networks and semiconductor device modeling. Together with E. Vittoz and F. Krummenacher, he is the developer of the EKV MOS transistor model.

Energy Limits in Current A/D Converter Architectures

Driven by ever-increasing application demands, the energy expended per A/D conversion has been reduced substantially over the last decade. This presentation surveys the most recent trends and investigates energy limits as they apply to A/D converter architectures commonly employed in fine-line CMOS technology (Flash, Pipeline, SAR and Oversampling Converters). Through this analysis, opportunities for further improvements are identified and discussed in detail, specifically emphasizing the impact of technology scaling.

Instructor: Boris Murmann is an Associate Professor in the Department of Electrical Engineering, Stanford, CA. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. Dr. Murmann's research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. He is a member of the International Solid-State-Circuits Conference (ISSCC) program committee, an associate editor of the IEEE Journal of Solid-State Circuits and a Distinguished Lecturer of the IEEE Solid-State Circuits Society.

Power Limits for Amplifiers and Filters

Increasing power consumption in amplifiers increases the speed and also reduces noise and distortion. The most common operational amplifiers, g_m blocks and wideband amplifiers are compared using a power-based FOM. Also discussed are continuous-time filters, switched-capacitor filters and G_mC filters. They are classified and compared based on a unified FOM. Again power is optimized in view of speed, noise and distortion.

Instructor: Willy Sansen received a PhD degree from U.C. Berkeley in 1972. Since 1980 he has been full professor at the Catholic University of Leuven, in Belgium, where he has headed the ESAT-MICAS laboratory on analog design up till 2008. He has been supervisor of sixty-four PhD theses and has authored and coauthored more than 650 publications and fifteen books among which the Powerpoint slide based book "Analog Design Essentials" (Springer 2006). He was Program chair of the ISSCC-2002 conference and President of the IEEE Solid-State Circuits Society in 2008-2009. He is the recipient of the D.O.Pederson award of the IEEE Solid-State Circuits in 2011. He is a Life Fellow of the IEEE.

Low-Power and Low-Voltage DC-DC Converter Design

With the recent advanced development of the VLSI system, power management circuits will be operated with lower output power requirement and with lower supply voltage. Several strategies to improve the power efficiency of low-power DC-DC converter are described and their pros and cons are discussed. Different design techniques for low-voltage dc-dc converter design are also included.

Instructor: Philip Mok is a Professor at the Department of Electronic and Computer Engineering, the Hong Kong University of Science and Technology in Hong Kong. He received his PhD in Electrical and Computer Engineering from the University of Toronto, Toronto, Canada, in 1995. His current research interests include power management integrated circuits and low-voltage analog integrated circuits design.