The Development of Large-Area Psec TOF Systems

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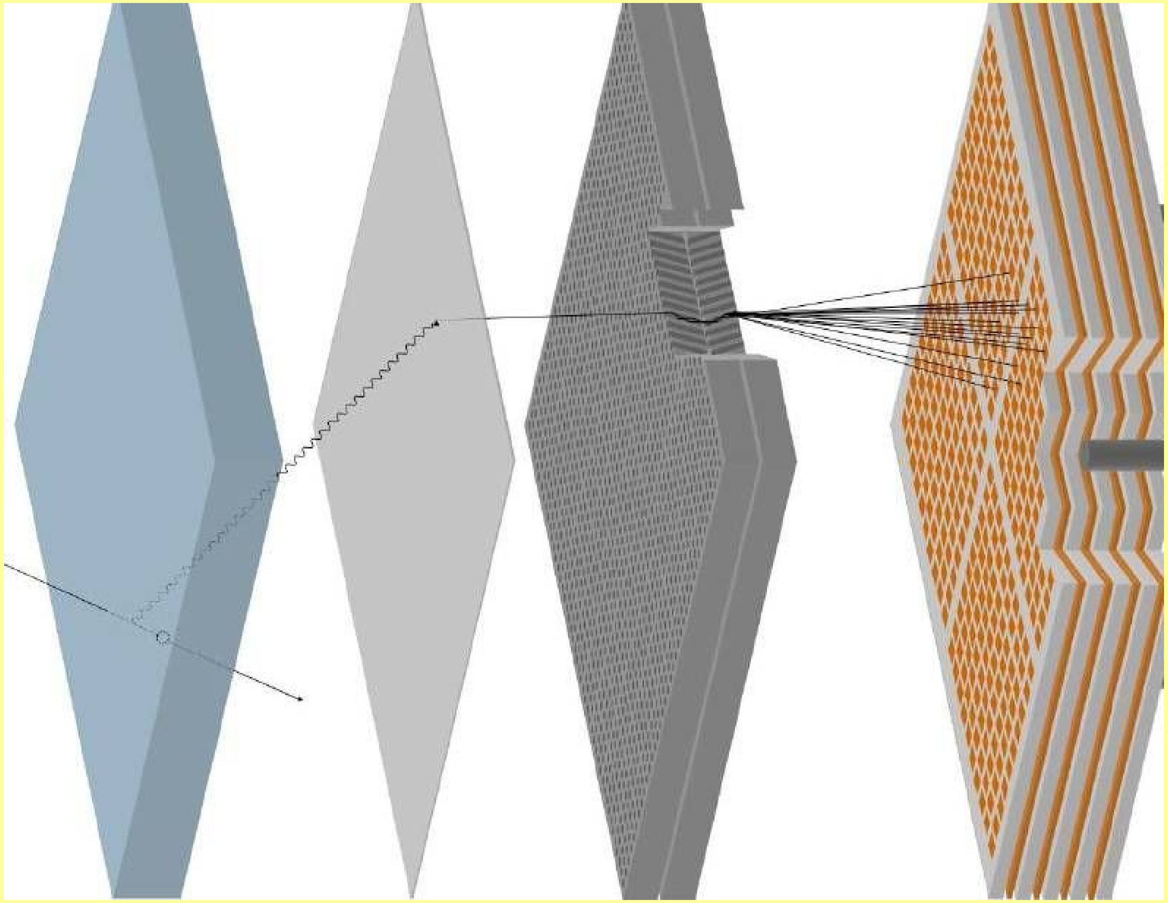


Introduction

- Time resolution hasn't kept pace- not much changed since the 60's in large-scale TOF system resolutions and technologies (e.g CDF-II upgrade resolution ~ 100 psec)
- Improving time measurements is fundamental , and can affect many fields: particle physics, medical imaging, accelerators, astro and nuclear physics, laser ranging, ….
- Need to understand what are the limiting underlying physical processes- e.g. source line widths, photon statistics, e/photon path length variations.
- Resolution on time measurements translates into resolution in space, which in turn impact momentum and energy measurements.

Collaborators on MCP development

Over-lapping mostly informal working together through work-shops, regular weekly meetings, blog, web page, 2 elogs, 2 workshops/year **http://hep.uchicago.edu/psec**

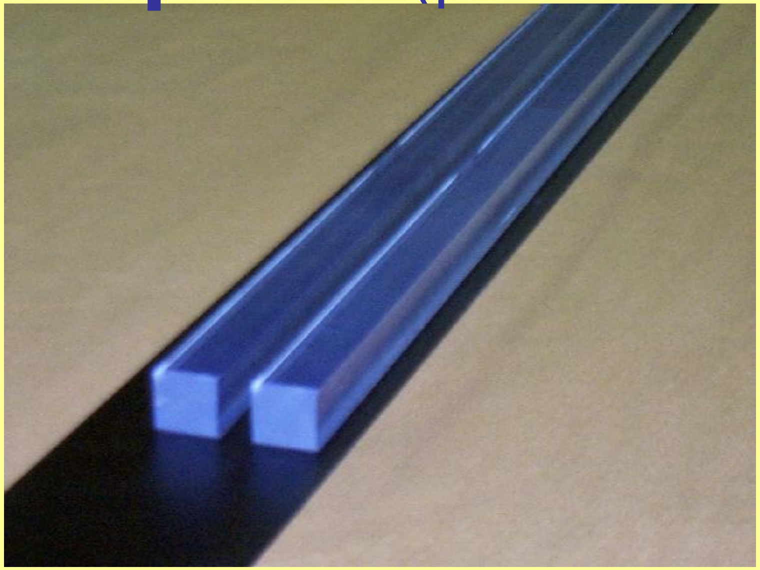
Take Fermilab P-979 list, e.g.:

- **Chicago: Jean-Francois Genat, Fukun Tang, Rich Northrop, Tyler Natoli, Heejong Kim, Scott Wilbur (Camden Ertley, Tim Credo)**
- **ANL: Karen Byrum, John Anderson, Gary Drake, Ed May**
- **Fermilab: Mike Albrow, Erik Ramberg, Anatoly Rhonzin, Greg Sellberg**
- **Hawaii: Gary Varner (sampling electronics)**
- **Saclay: Patrick Ledu (now Lyon), Christophe Royon**
- **SLAC: Jerry Va'vra**

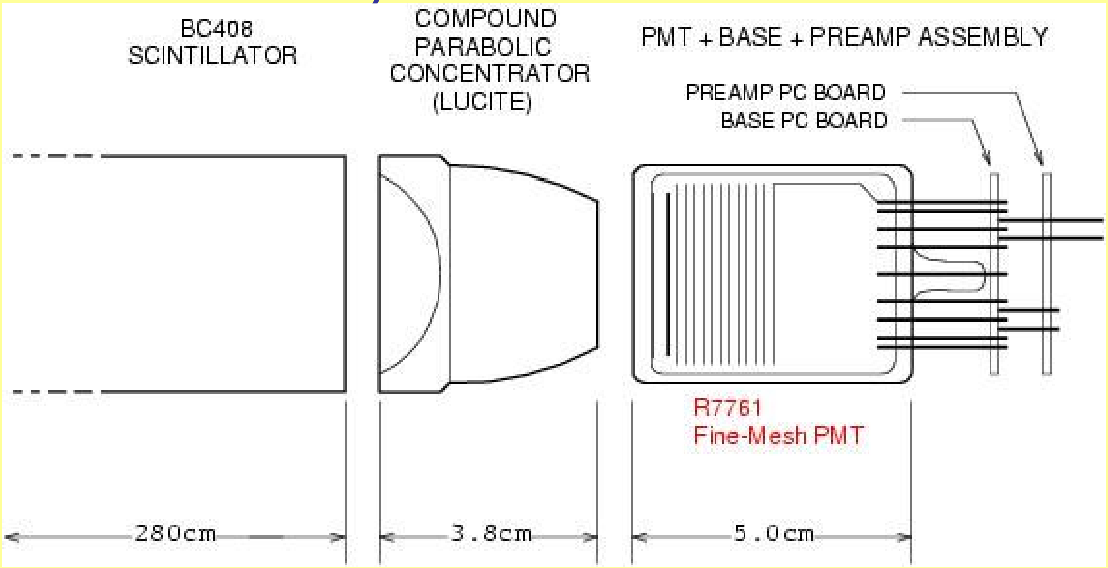
Why has 100 psec been the # for 60 yrs?

Typical path lengths for light and electrons are set by physical dimensions of the light collection and amplifying device.

These are now on the order of an inch. One inch is 100 psec. That's what we measure- no surprise! (pictures from T. Credo)



Typical Light Source (With Bounces)



Typical Detection Device (With Long Path Lengths)

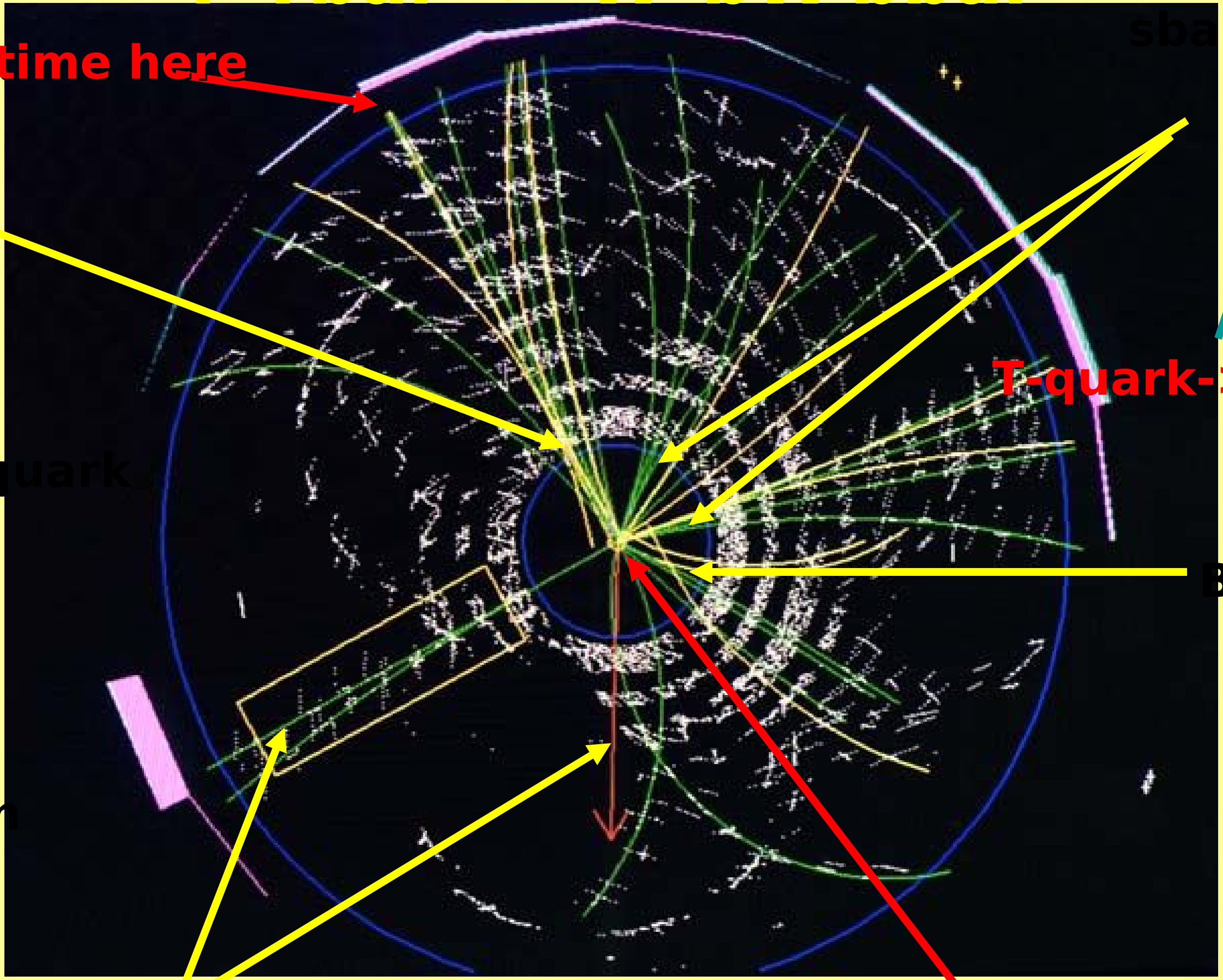
A real CDF Top Quark Event

T-Tbar -> W^+bW^-bbar

W->charm
sbar

easure transit time here
top)

B-quark



T-quark->W+bquar

-quark->W+bquark

B-quark

Cal. Energy
From electron

W->electron+neutrino

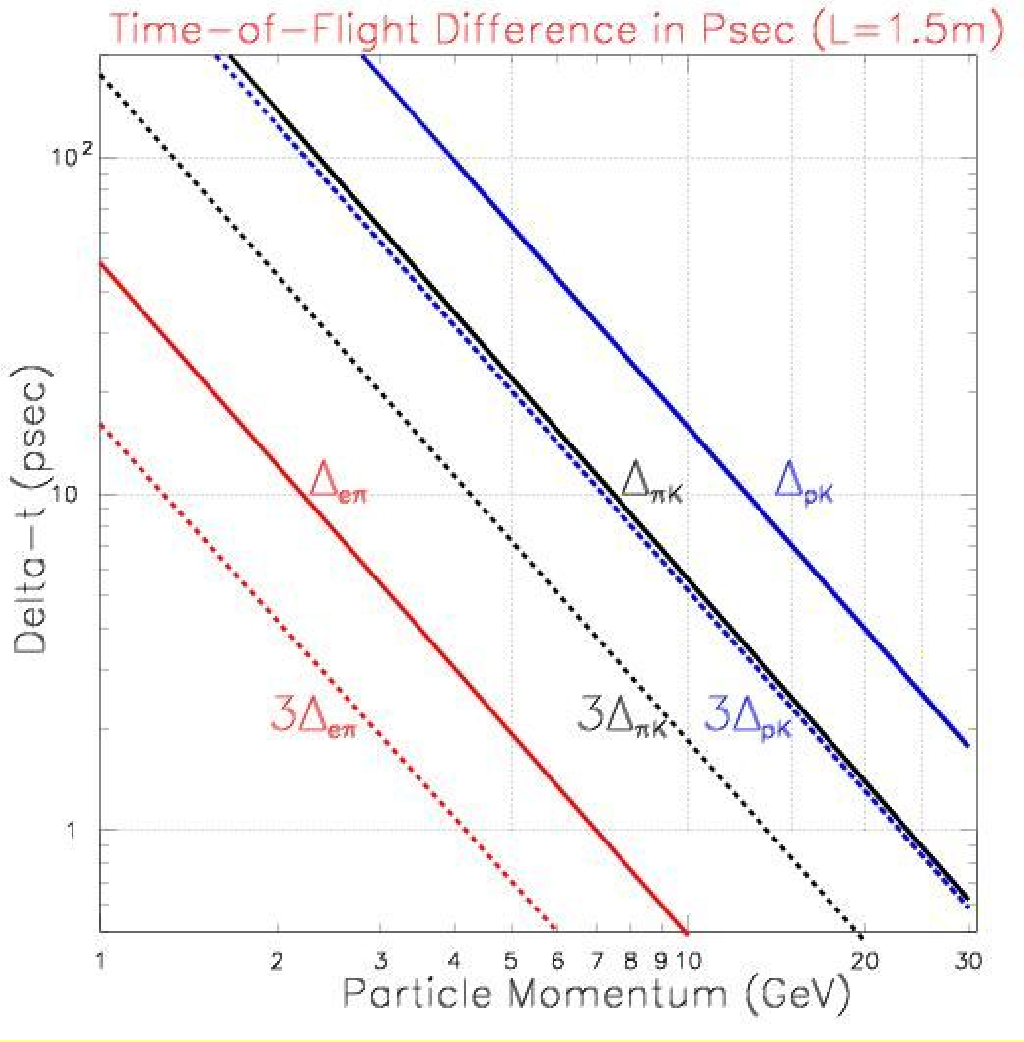
Fit t_0 (start) from all tracks

follow the color flow through kaons, cham, bottom?

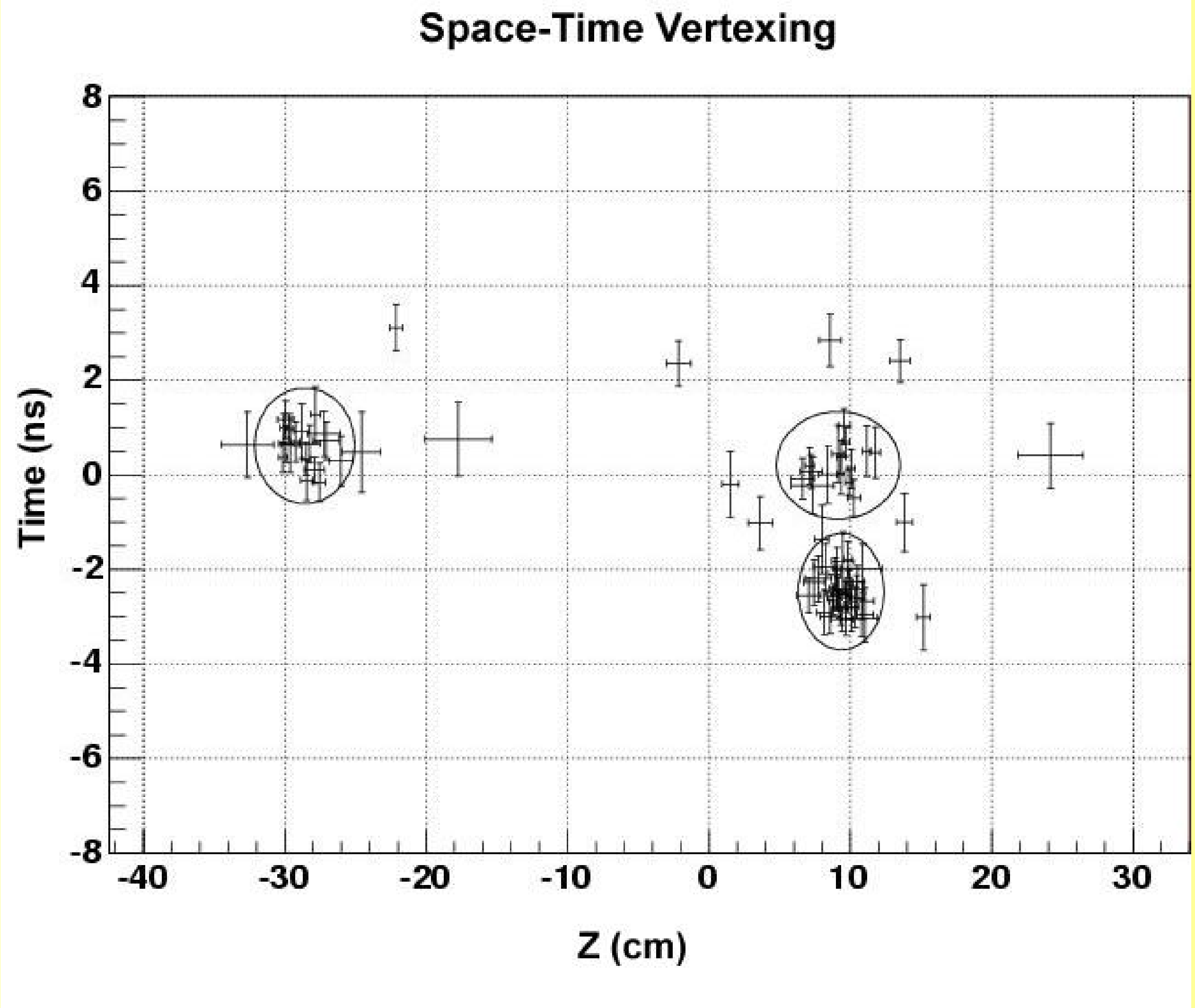
Resolution- want 1-few psec (!).

W-mass: W->c+sbar or u+dbar- different kaon production

Top-mass: t+tbar -> W+W-b+bbar: need to tell b from



Photon Vertexing



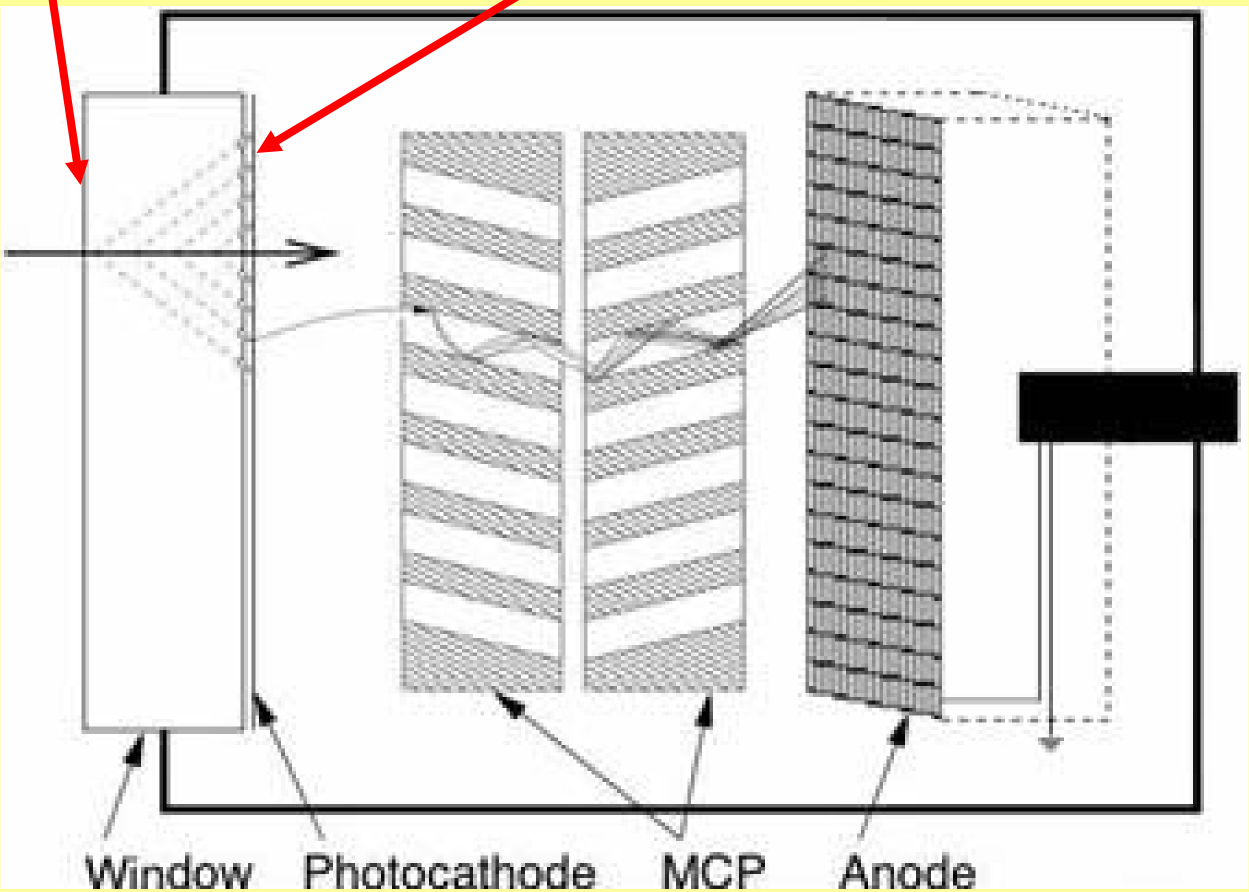
- Atlas Upgrade- Higgs to gamma-gamma?

Generating the signal

Use Cherenkov light – fast- no bounces.

Incoming rel. particle

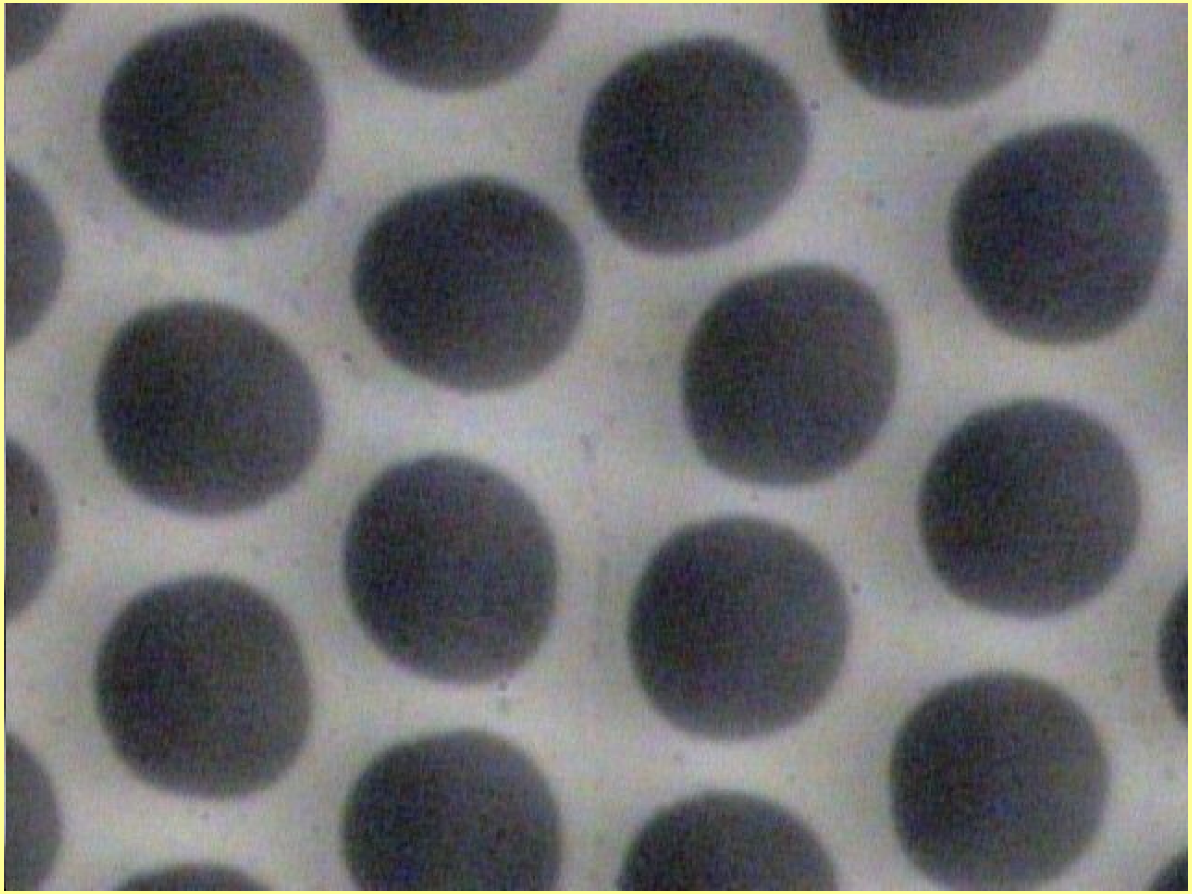
Photo-cathode



A 2” x 2” MCP- actual thickness ~3/4”

e.g. Burle (Photonis) 85022-with mods per our work

Started with off-the shelf commercial (Burle) MCP's*

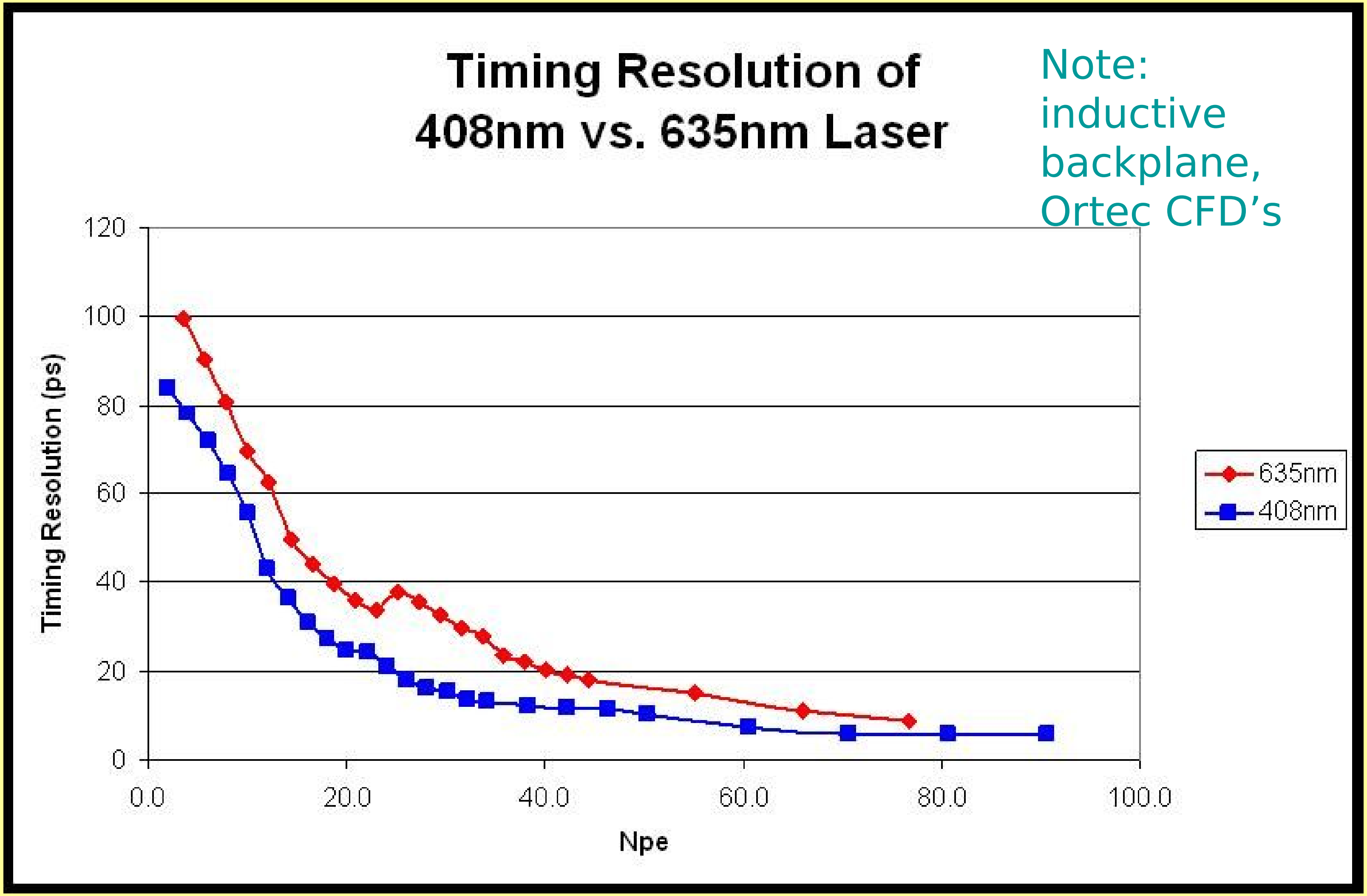


25-micron 2" square Planicon (Photonis/Burle)-

Micro-photograph by Greg Sellberg at Fermilab

***After considering other devices- MCP's are in principle scaleable in area.**

ANL laser-test stand and commercial Burle 25-micron tube results (Camden Ertley)



Note: inductive backplane, Ortec CFD's

Understanding the contributing factors to 6 psec resolutions with present Burle/Photonis/Ortec setups- Jerry Vavra’s Numbers

1. TTS: 3.8 psec (from a TTS of 27 psec)
2. Cos(theta)_cherenk 3.3 psec
3. Pad size 0.75 psec
4. Electronics 3.4 psec

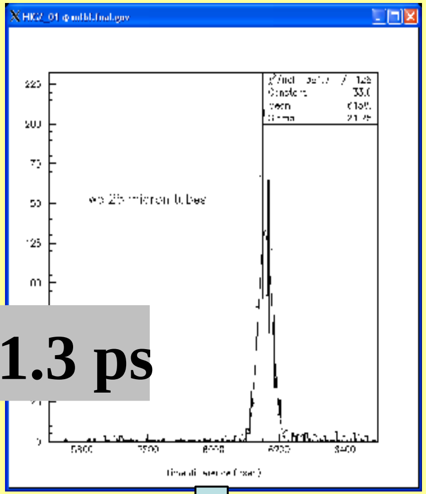
PSEC Test Beam Folks

Have had 2 runs at Fermilab MTEST beam- mostly 120 GeV protons

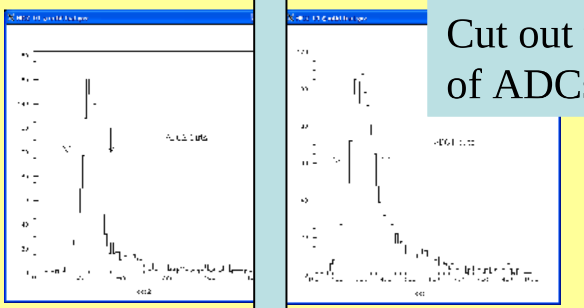
Get ~15 psec, in ~agreement with simulations (more on this later).

Results from Photonis 25 μm Pore MCP/PMT

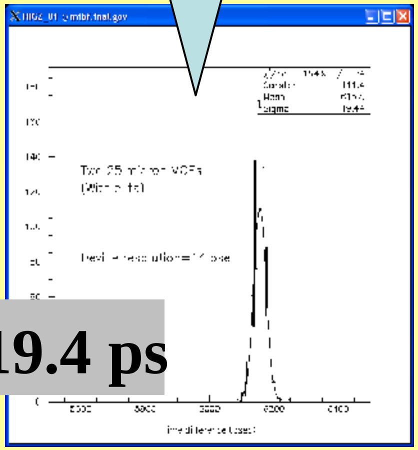
(Eric Ramberg Slide)



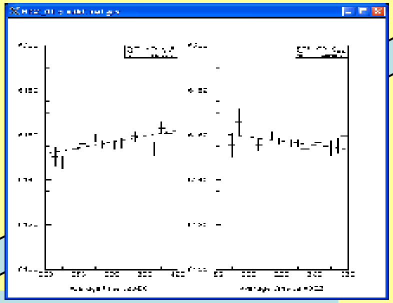
σ_t= 21.3 ps



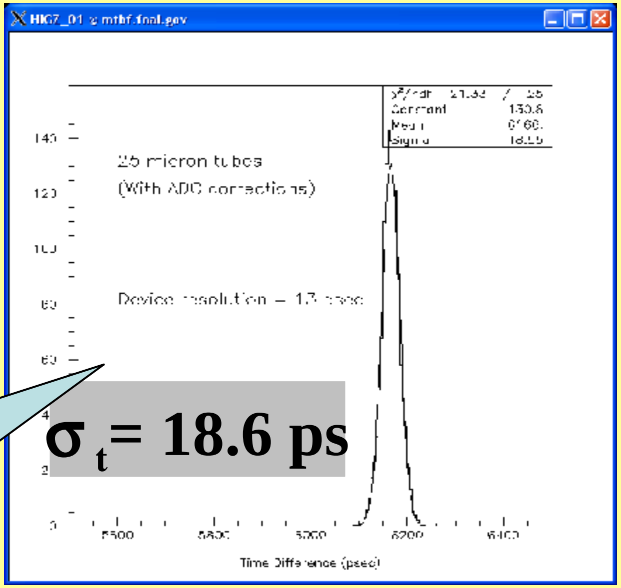
Cut out tails of ADCs



σ_t= 19.4 ps



Apply small PH slewing correction



σ_t= 18.6 ps

σ_t(device+noise) = 13.1 ps

σ_t = 12.3 ps

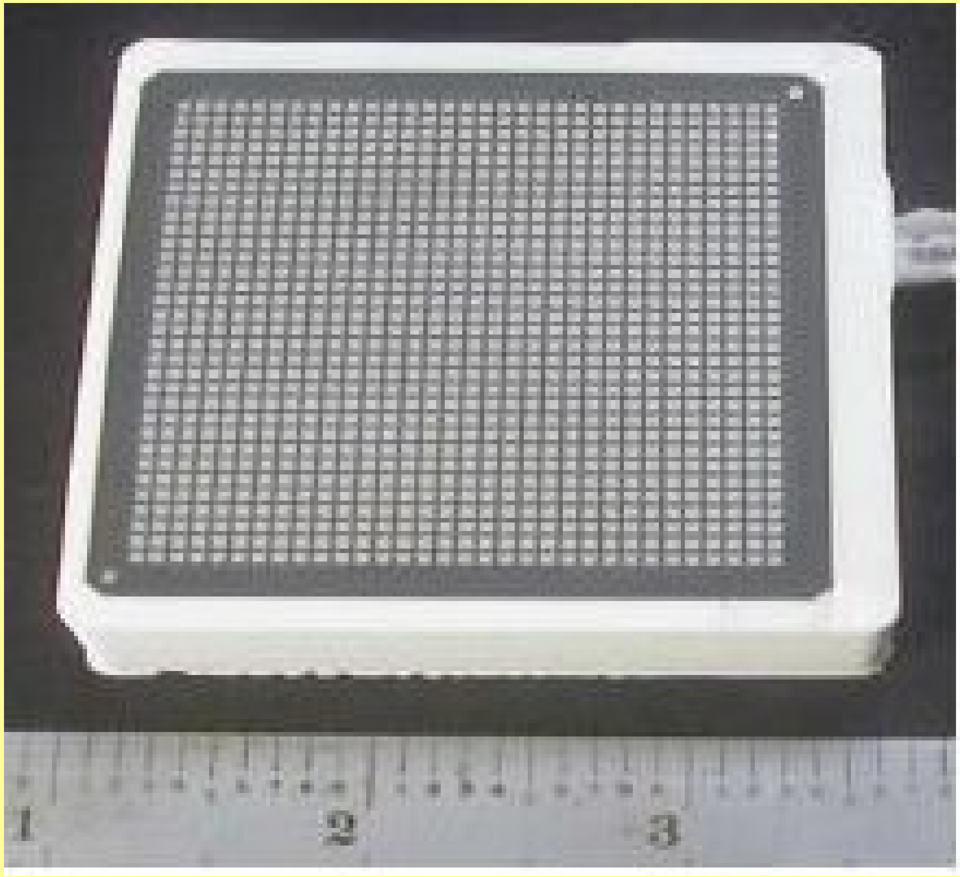
25 micron-pore tube => 3-400 psec rise time

TTS and Rise Time vs Pore Size

- We are all set now to compare 2 MCP's that are identical except with 10 micron and 25 micron pores in laser test stand (compared in beam test but…)
- Literature gives factor of 4 difference in rise time between 25 and 10 micron; 6 micron and 3 micron faster yet.
- We would like to be able to reproduce this in simulation as well in tests- question- how far down can you go (see later)?

Collecting the signal

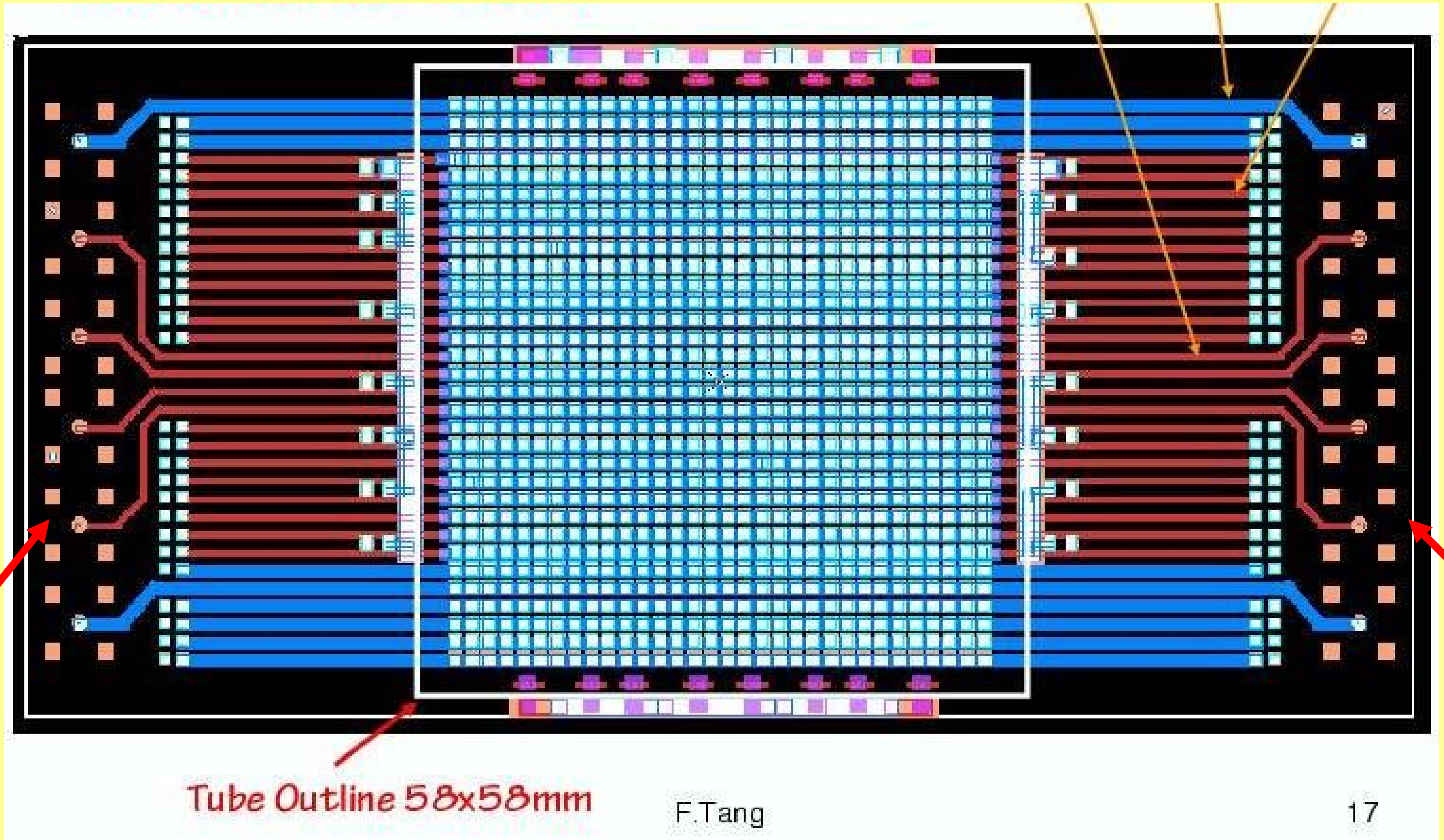
- We are using 1024-anode 2”x2” Photonis MCP’s.



Collecting the signal

Get position AND time

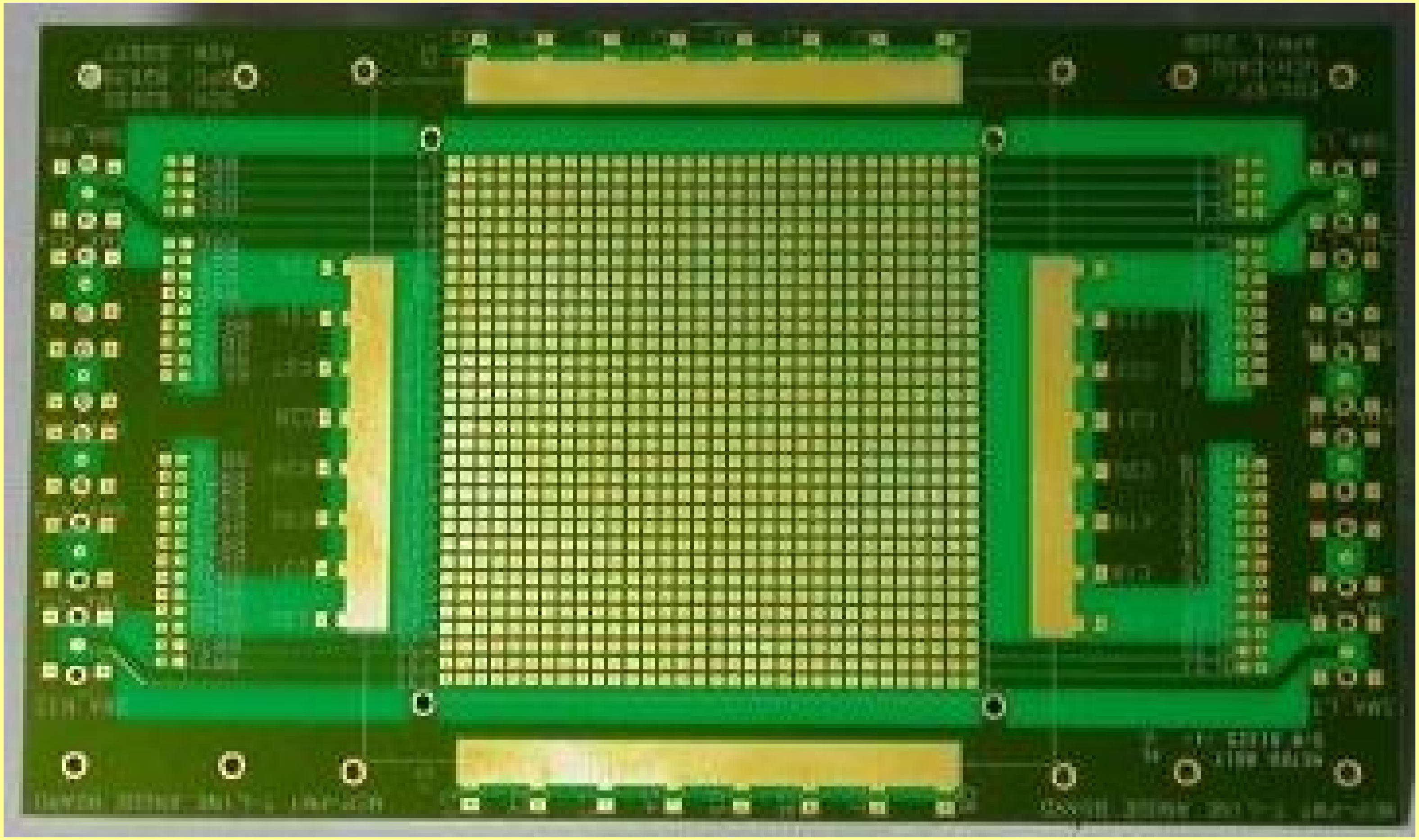
Anode Design and Simulation (Fukun Tang)



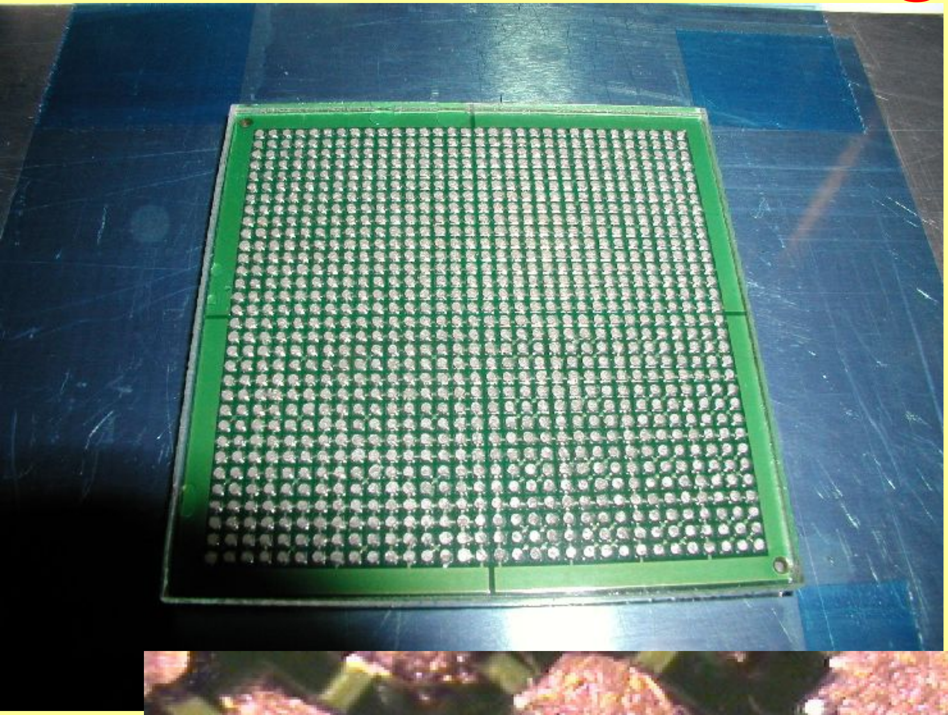
- Transmission Line- readout both ends=> pos and time
- Cover large areas with much reduced channel account.

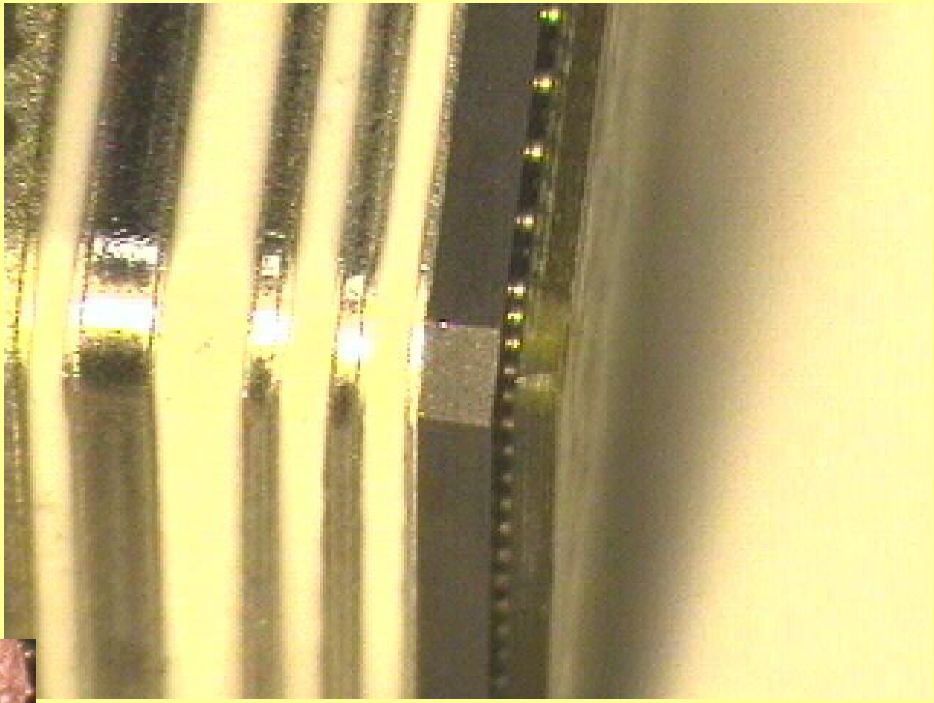
Collecting the signal

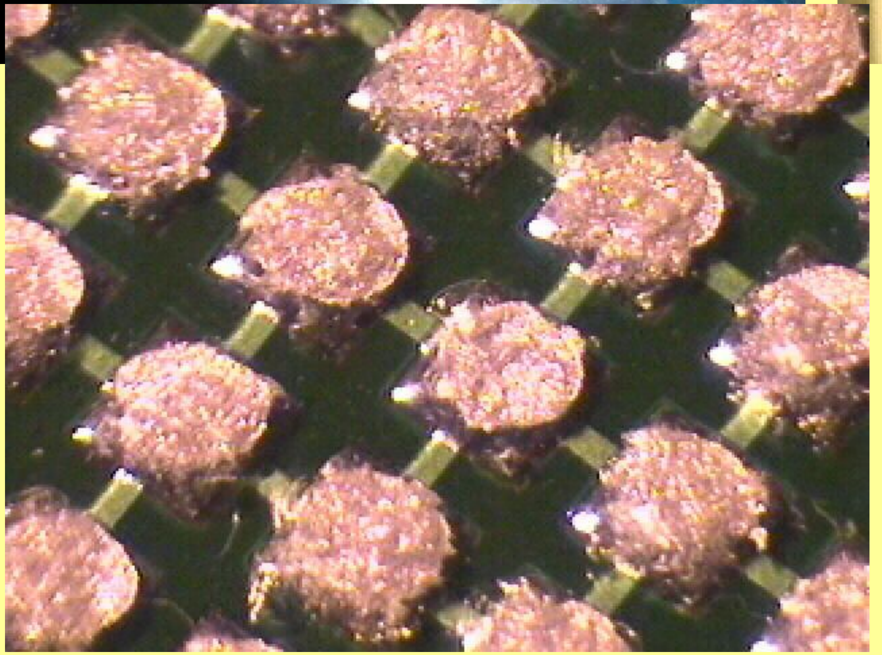
- 50-ohm Transmission-line PC card



Collecting the signal

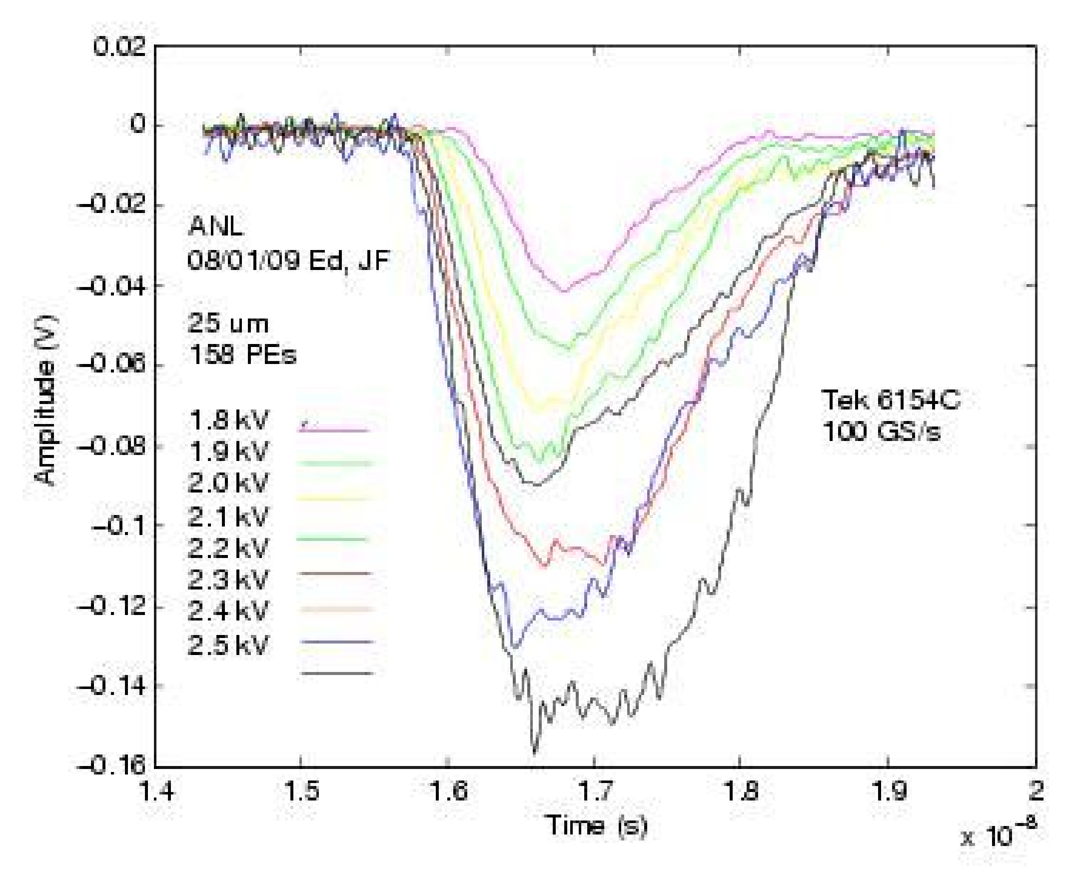






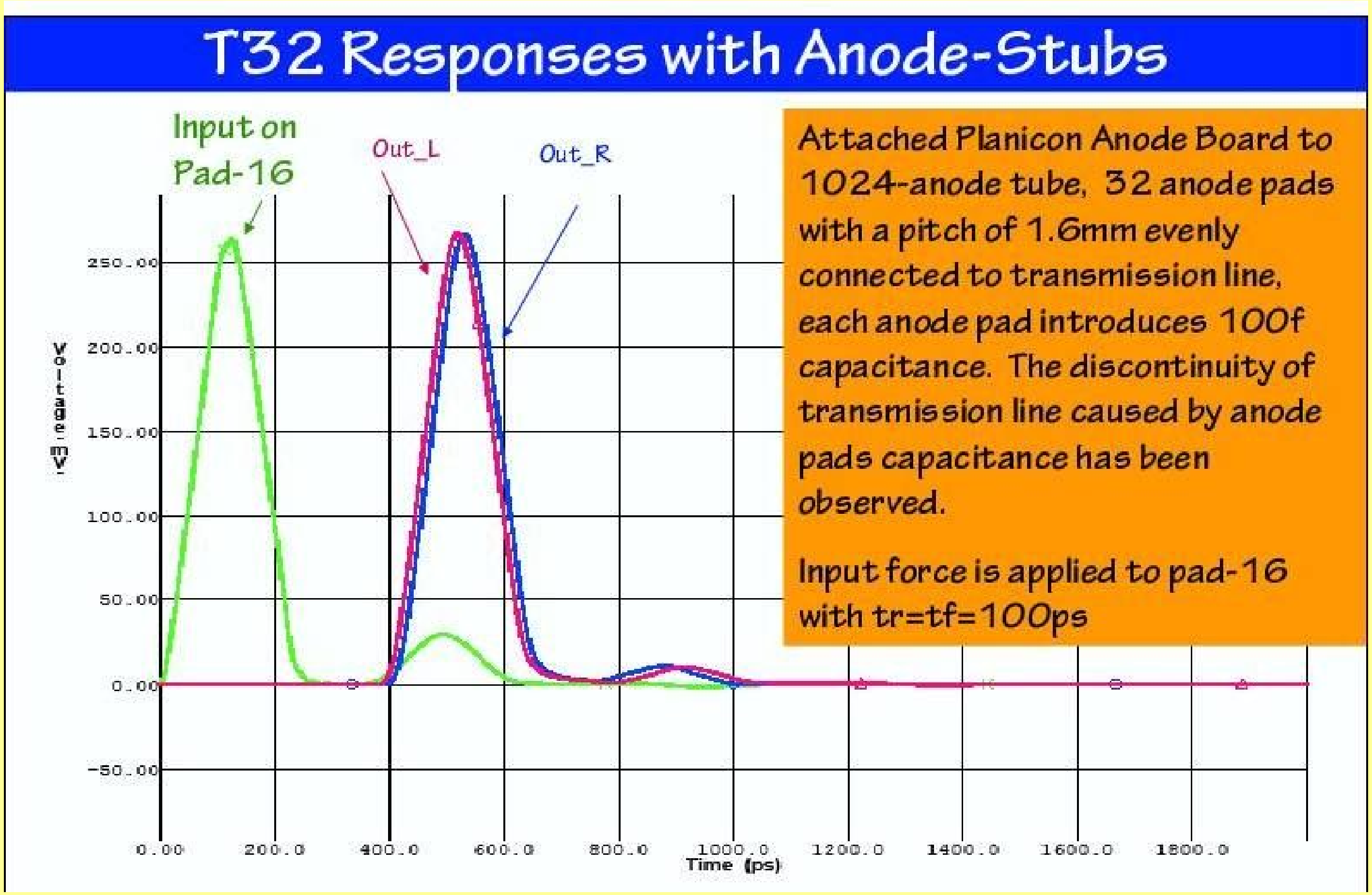
Conducting epoxy- using Stencil- Quik (BEST)

Collecting the signal



Collecting the signal

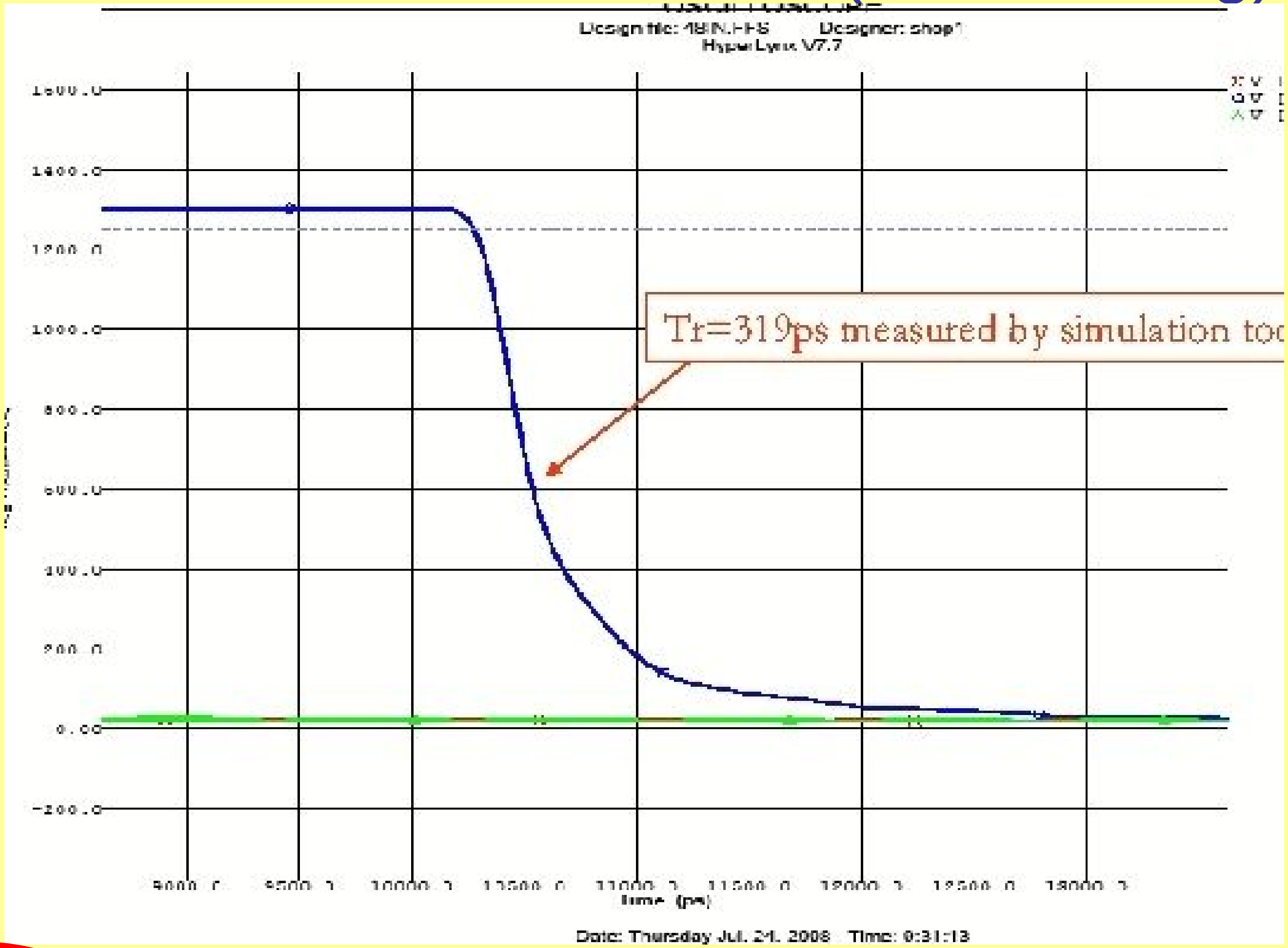
Anode Design and Simulation(Fukun Tang)



- Transmission Line- simulation shows 3.5GHz bandwidth- 100 psec rise (well-matched to 10-micron pore MCP)

Scaling Performance to Large Area

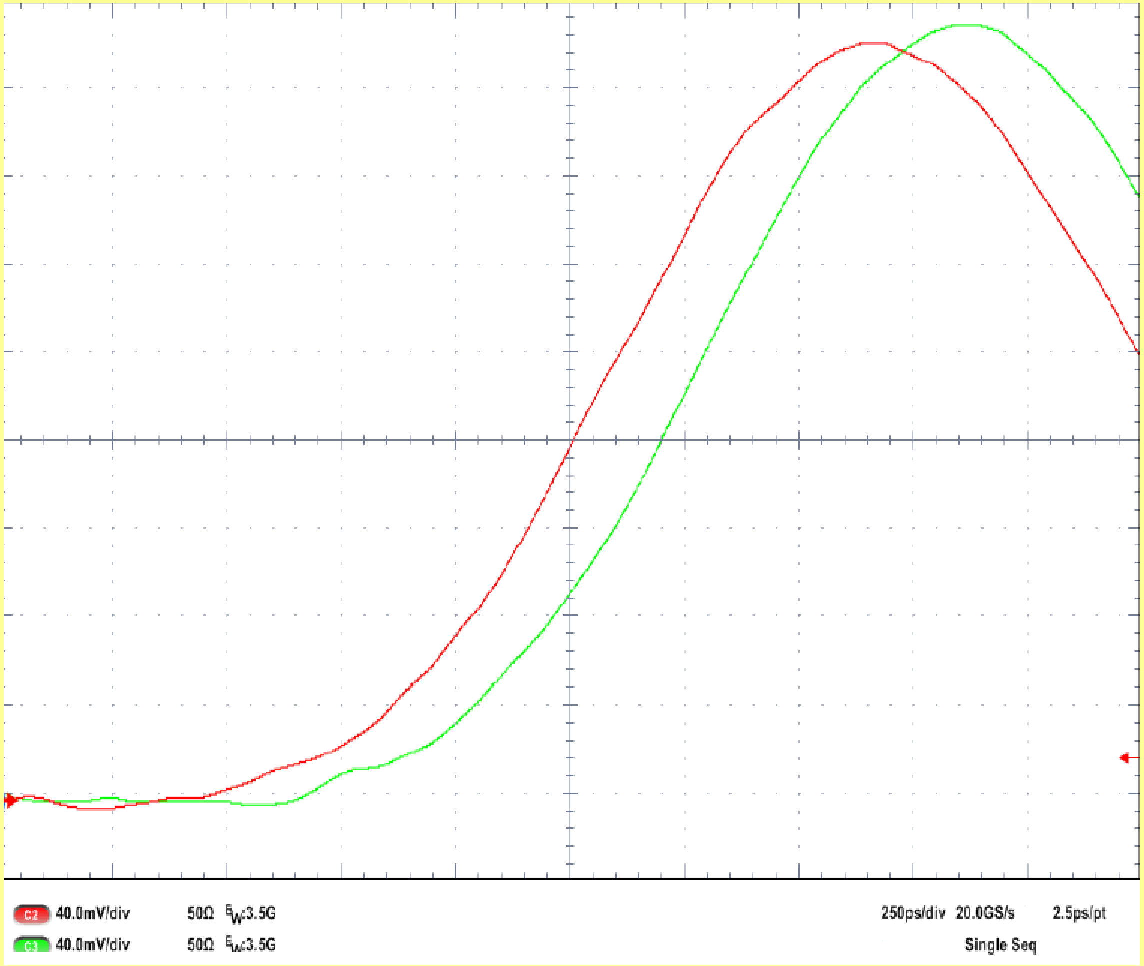
Anode Simulation(Fukun Tang)



- 48-inch Transmission Line- simulation shows 1.1 GHz bandwidth- still better than present electronics.

Collecting the signal

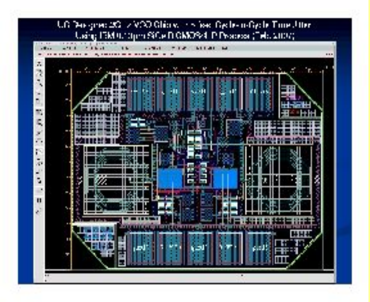
Measurement of the transmission line propagation velocity. The horizontal time scale is 250 psec/div; the pulser rise time is 900 psec. The difference in signal paths is 3.5 cm. (from Jean-Francois Genat). [note typical MCP risetimes are 60-300 psec).



Front-end Electronics

Critical path item- probably the reason psec detectors haven't been developed

- We had started with very fast BiCMOS designs- IBM 8HP-Tang designed two (really pretty) chips
- Realized that they are too power-hungry and too 'boutique' for large-scale applications
- Have been taught by Gary Varner, Stefan Ritt, Eric DeLanges, and Dominique Breton that there's a more clever and elegant way- straight CMOS – sampling onto an array of capacitors
- Have formed a collaboration to do this- have all the expert groups involved (formal with Hawaii and France)- see talks by Tang and Jean-Francois



Digitizing the signal

- We started on the electronics with a very fast (200 GHz) IBM BiCMOS process (8HP)- idea was to make a `time-stretcher' and then it becomes a known problem
- 8HP is very expensive, limited access, and high power. We made one chip at IHP, and one design at IBM, and bailed out.
- Based on detailed simulations, we think waveform sampling with CMOS will work

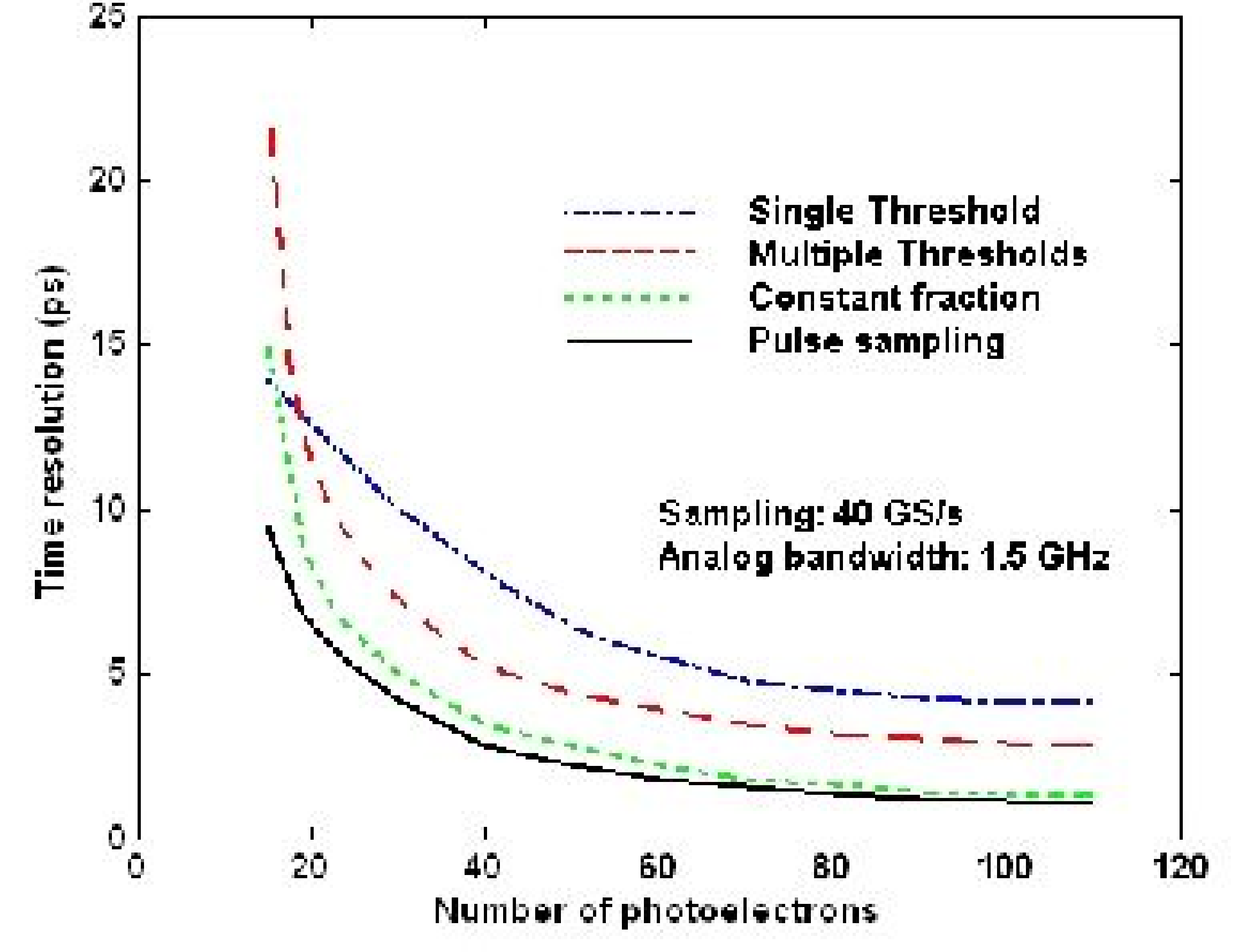
Digitizing the signal

Use MCP signals captured by our fancy sampling scope (15 GHz abw) as input to simulation- compare different timing techniques (Genat, Varner, Tang and HF; arXiv 0810.5590)

Technique	Resolution (ps)
Leading Edge	**7.1**
Multiple Threshold	**4.6**
Constant Fraction	**2.9**
Waveform Sampling	**2.3**

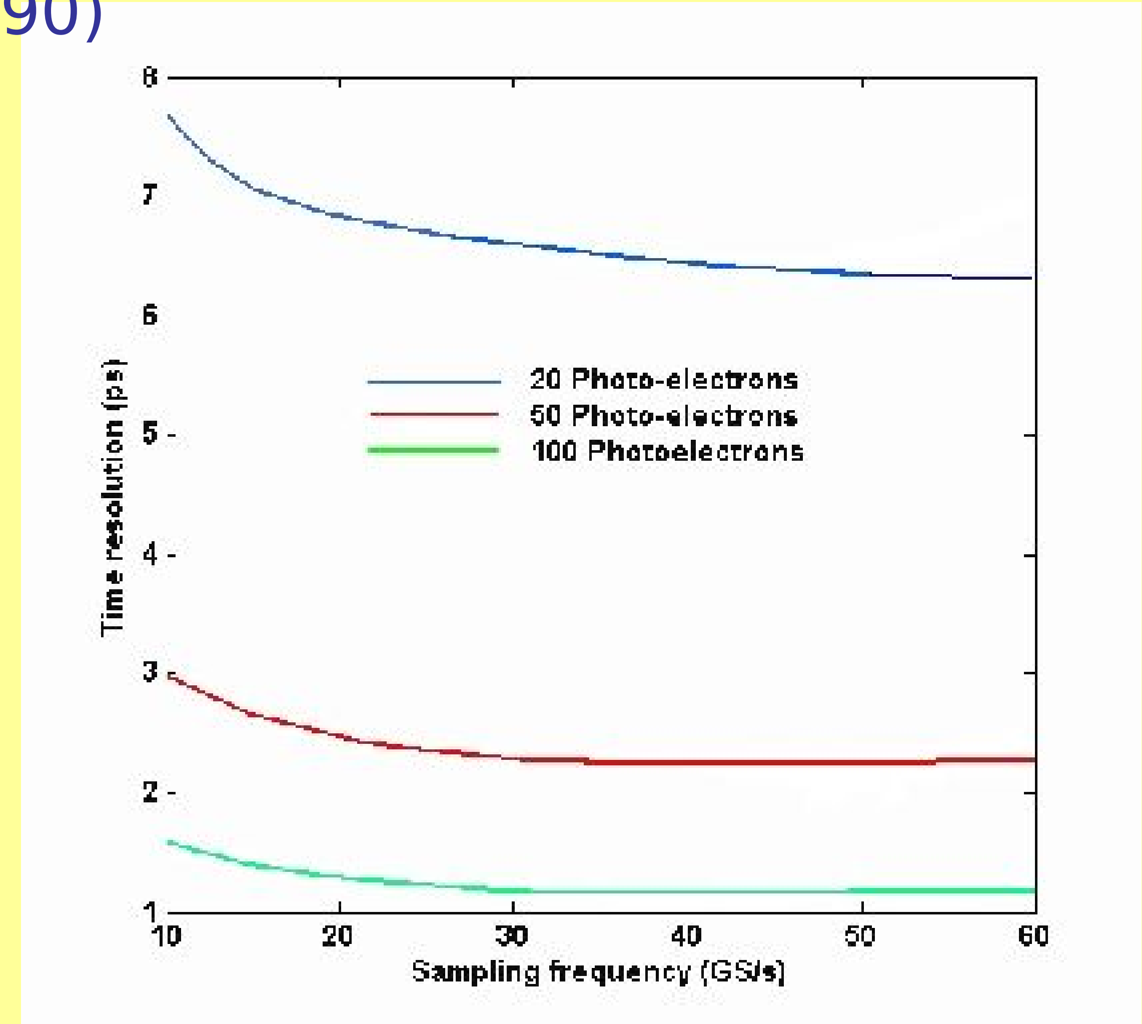
Digitizing the signal

Use simulation based on scope data to compare four methods of time measurement:



Digitizing the signal

Time Resolution depends most strongly on three parameters: ABW, S/N, and Signal Size. (Genat, Varner, Tang and HF; arXiv 0810.5590)

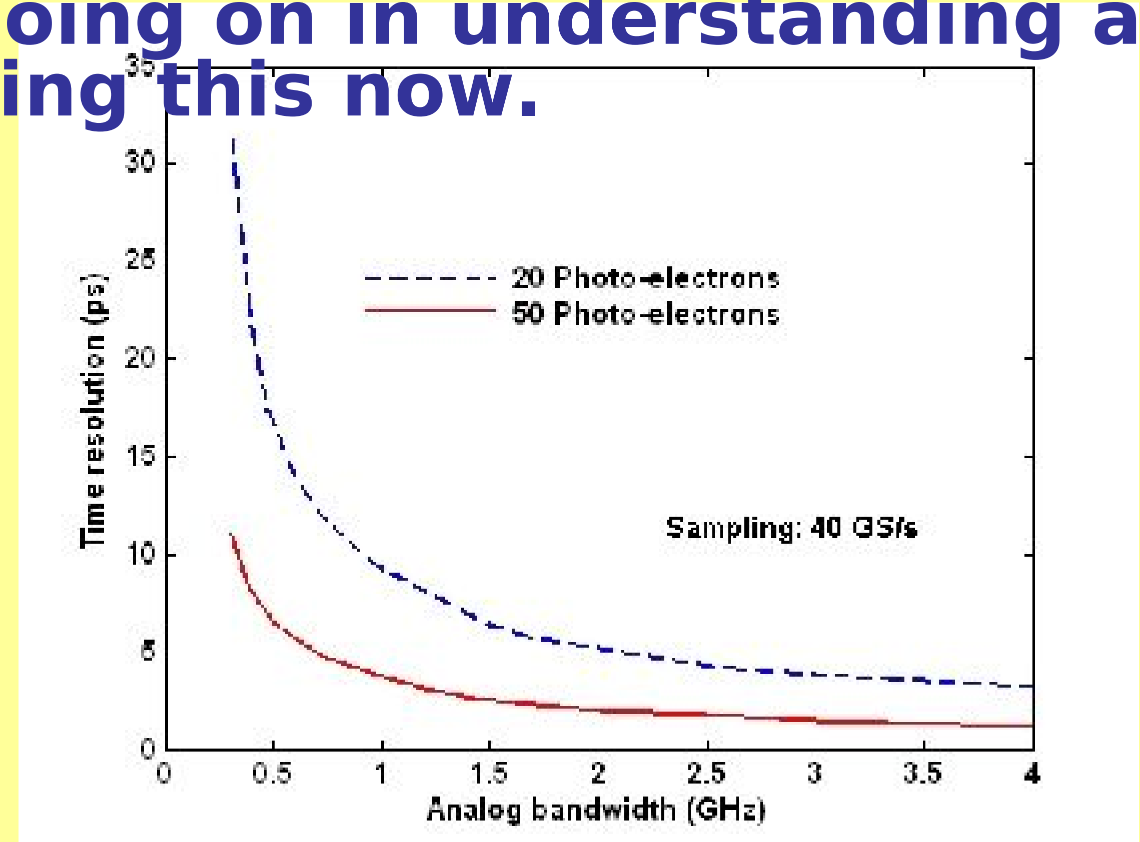


Also have simulated sampling jitter, number of bits- need only 8 bits

Expect ~50 PE's from Cherenkov light in 1 cm in fused quartz

Digitizing the signal

The analog band-width into the sampling chip is a key parameter. The PC card has high ABW (3.5 GHz), but it's not easy to make a high ABW CMOS sampler. Much effort going on in understanding and simulating this now.



Plot of resolution vsABW; we hope we can get 1.5 GHz in 0.13 micron.

Status of Sampling Effort

1. Have sample chips and demo bds of DRS4 chip from Stefan Ritt (PSI)- under test with MCP's and transmission line card. (Have offset 4 channels to get 20 GS/sec).
2. Working with Gary Varner on plan to use one of his designs on the next version of the transmission line PC card.
3. Collaborating with Dominique Breton and Gary on a 40-GS/sec chip in IBM 8RF (0.13 micron).

II STATE OF THE ART

Several circuits have already been designed in the HEP community for fast pulse sampling, mainly to record photo-multipliers pulse shapes. As detailed in section I, fast timing requires higher sampling rates, but smaller dynamics ranges.

	Hawaii		Orsay/Saclay		PSI		PSEC
	Lab 3	Planned Blab2	Sam	Planned	DRS3	Planned DRS4	This proposal
Sampling frequency	20 MHz-3.7 GHz	1-10 GHz	0.7-2.5 GHz	10 GHz	10 MHz-5 GHz	5 GHz	40 GHz
Analog bandwidth	900 MHz	850 MHz	300 MHz	650 MHz	450 MHz	> DRS3	>1 GHz
Number of Channels	9	16	2		12/6/2/1	8/4/2/1	16
Triggered mode	Common Stop	Channel trigger on sums	Common Stop		Common Stop	Common Stop	Channel trigger
Resolution		10 bit	11.6 bit		11.6 bit	11.5 bit	8-10 bit
Samples	256	4/8 rows of 512	256	2048	1024-12288	1024-8192	64
Clock	33 MHz	33 MHz	66 MHz		20 MHz	fsamp/2048	60 MHz
Max latency			5ms		0.6 ms		
Input Buffers		TIA (5kOhm gain)	Yes	No	No	No	Yes
Differential Inputs	No	Pseudo-diff	Yes		Yes	Yes	Pseudo diff
Input impedance	50 Ohms Ext	30-70Ohms adjustable	> 10 MOhm			7-11pF	
Readout clock		1 GHz Wilkinson	16 MHz		33 MHz	33 MHz	60 MHz
Readout time	150µs	512µs	< 2 µs		30ns * [illegible] samples	30ns * [illegible] samples	< 1 µs
Locked delays	Ext DAC	Ext DLL	Int DLL		Ext PLL	Int PLL	
On-chip ADC	Yes	1 GHz Wilkinson	No		No	No	Yes
R/W simultaneous		Yes	No		No	Yes	No
Power/ch	50mW	20mW/sample 0.2W/read	150 mW		1-13mW	2-20mW	
Dynamic range		1mV/1V	0.65mV-2V		0.35mV/1.1V	0.35/1V	1V
Xtalk	Average << 10%	< 0.1%	0.30%		<0.5%	<0.5%	
Sampling jitter		TBD	40ps		200ps (Ext [illegible])	Ext PLL	10ps
Power supplies	2.5V	2.5V	0-3.3V		2.5V	2.5 V	1.8V
Process	TSMC 0.25	TSMC 0.25	AMS 0.35	AMS 0.18	UMC 0.25	UMC 0.25	CMOS 0.13
Chip area	2.5 mm2	12 mm2	10 mm2		25 mm2	25 mm2	1 mm2
Cost/channel		500$/40 10$/2k	15.7$/12k			10-15$	

Table 1. State of the art, this proposal. The yellow column is from Gary Varner's group at the University of Hawaii (USA) [12], the light blue from Dominique Breton from the University of Paris-Sud (Orsay) [10] and Eric Delagnes from CEA (Saclay), (France) [11]. The orange column from Stefan Ritt at PSI (Switzerland) [13]. The dark blue is this proposal.

Jerry’s #’s re-visited : Solutions to get to <several psec resolution.

- **TTS: 3.8 psec (from a TTS of 27 psec)**

  MCP development- reduce TTS- smaller pores, smaller gaps, higher fields (- also different geometries?)

- **Cos(theta)_cherenk 3.3 psec**

  Same shape- spatial distribution (measure spot) (-also cleverness in light collecting?)

3. **Pad size 0.75 psec-**

   Transmission-line readout and shape reconstruction, but it’s small to begin with..

4. **Electronics 3.4 psec –**

   fast sampling- should be able to get < 2 psec (extrapolation of simulation to faster pulses)

New Topic-Are There Other Techniques to Make Psec Large-Area Detectors?

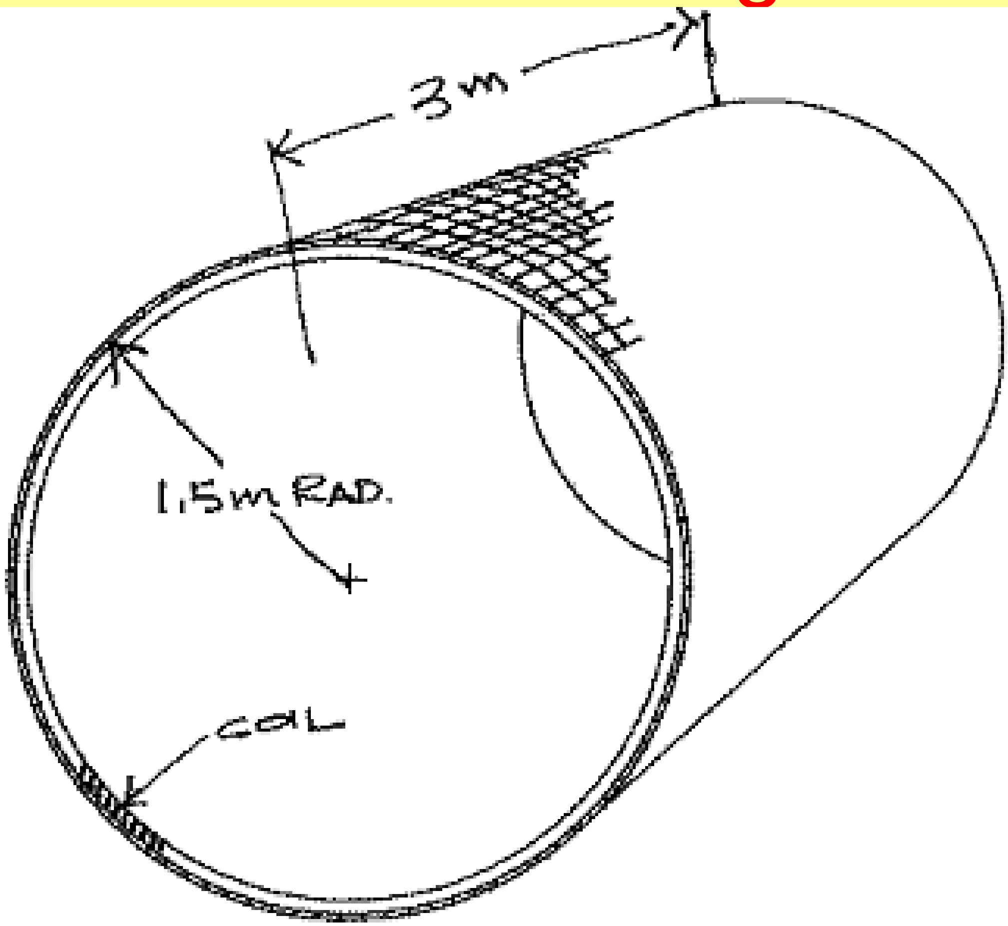
- Transmission-line readout allows scaling to big areas as one reads out only the ends of the lines (1.1 GHz at 48")
- Get time from the average of the 2 ends and position from the difference- 3D (`tomographic')- allows vertexing.
- Needs a `batch' fabrication process- something different.

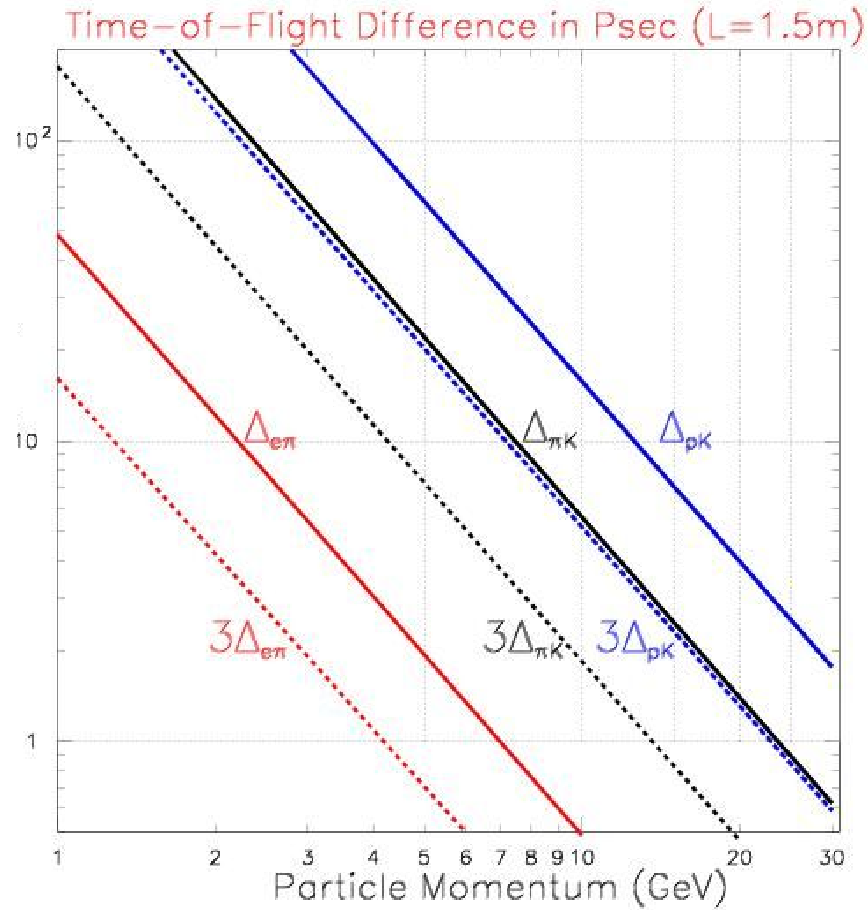
Not obviously impossible…

Large-Area Psec Detector Development- 3 Prongs:

1. Electronics- have settled on wave-form sampling at ends of long transmission lines (48” has 1.1GH ABW)
   - **Chips demonstrated by Breton, Delanges,Ritt, and Varner- many `pieces’ exist, main change in chip is going to faster process and pooling expertise**
2. MCP development- techniques and facilities
   - ALD, anodic alumina--will require industry, natl labs. Argonne has AAO, ALD, Center for Nano-scale Science, some amazing people. Rosner has offered a post-doc+funds to seed an effort. DOE is interested and (in words) supportive.
3. End-to-End Simulation (particle in–>digital data out)
   - **Electronics simulation in good shape**
   - **Rudimentary `end-to-end’ MCP device simulation exists-**
   - **Have recently discovered Valentin Ivanov (Muons.Inc)- SBIR**
   - **We can (and have) validate with laser teststand and beam line**

Application 1- Collider Detector Upgrade Charged Particle ID

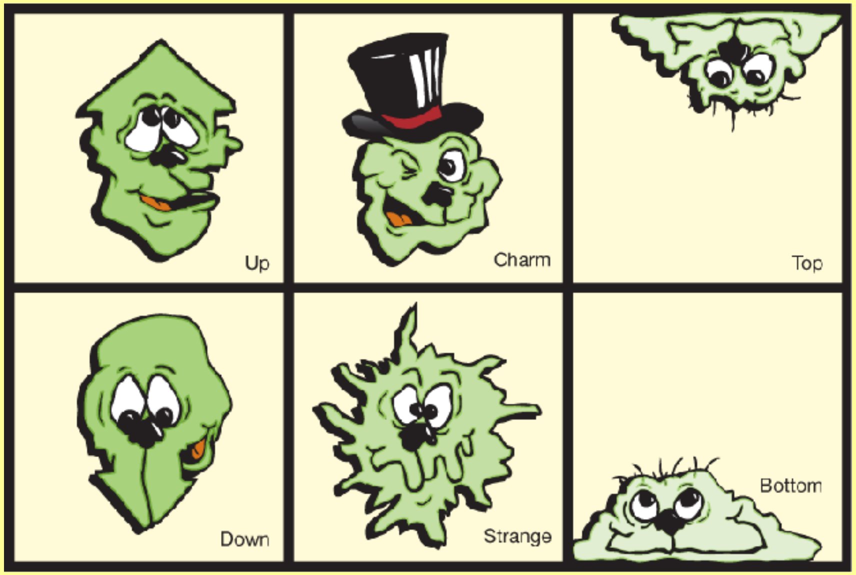




- E.g- Tevatron 3rd-generation detector (combine D0 and CDF hardcore groups); ATLAS Upgrade (true upgrade)

Application 2-Super-B Factories

- Particle ID for precision b-physics measurements in larger angle regions
- Probe energy frontier via precision/small σ
- Gary Varner and Jerry Va'vra, Nagoya working on it



Application 3: Fixed-target Geometries Particle ID and Photon Vertexing

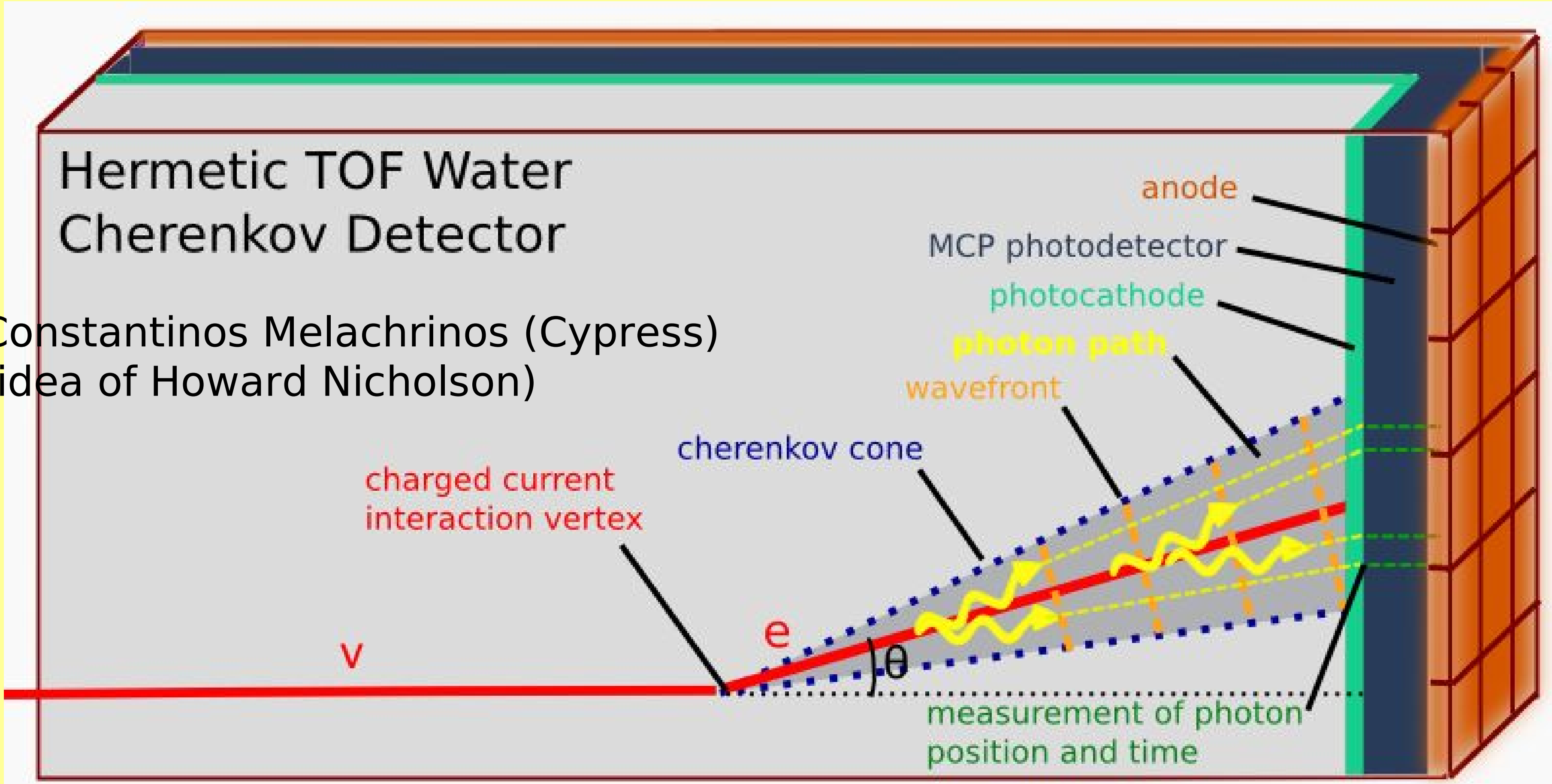
- - Consider LHCb and JPARC $K_L^o \rightarrow \pi^0 \nu\nu$

Geometry is planar- i.e. the event is projected onto a detection plane. Timing gives the path length from the point on the plane*-

Critical new information for vertexing, reconstruction of π^0 's from 2 photons, direction of long-lived particles.

Very thin in 'z'-direction, unlike Cherenkov counters.

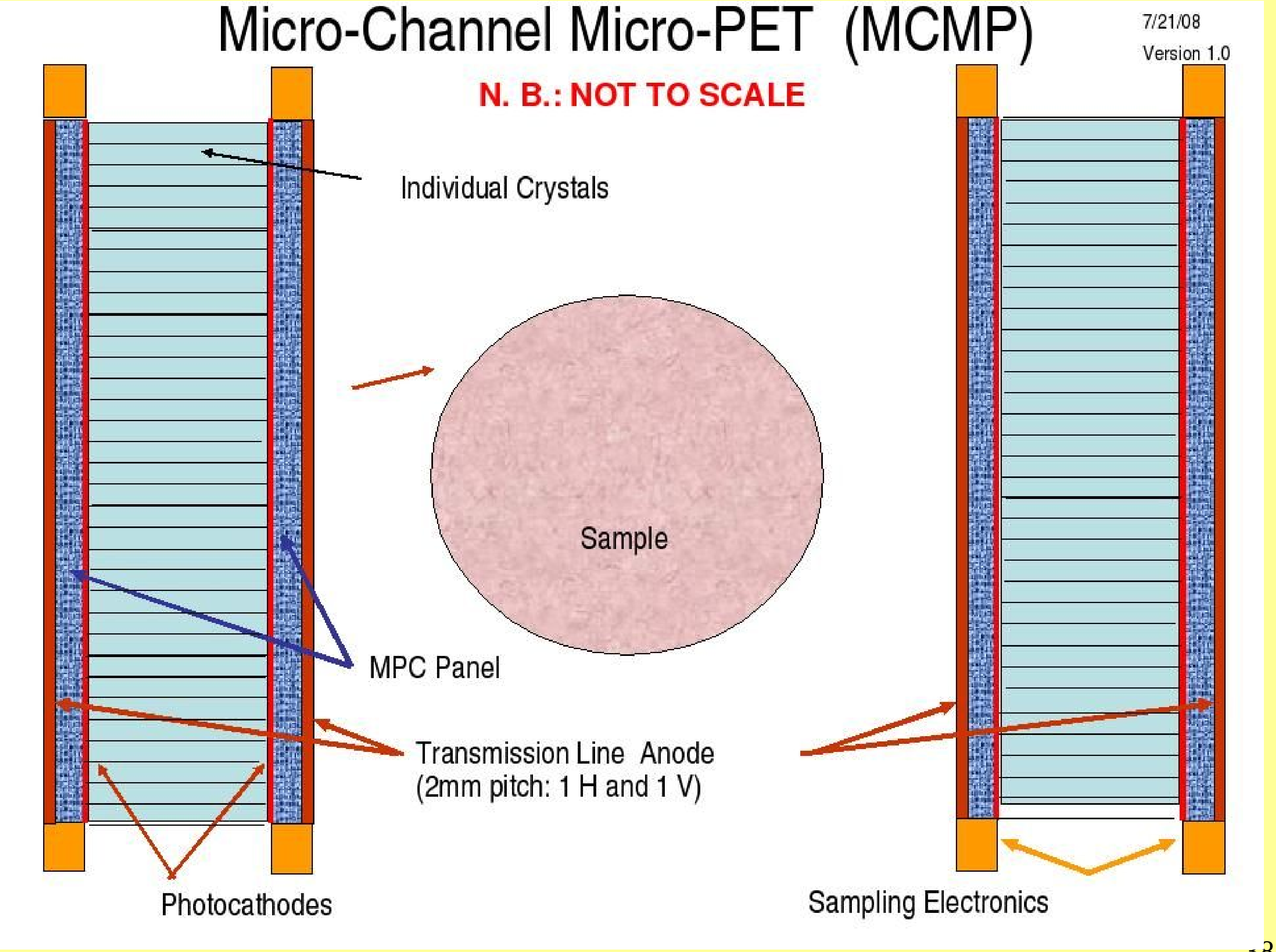
Application 4- Neutrino Physics



Constantinos Melachrinos (Cypress)
(idea of Howard Nicholson)

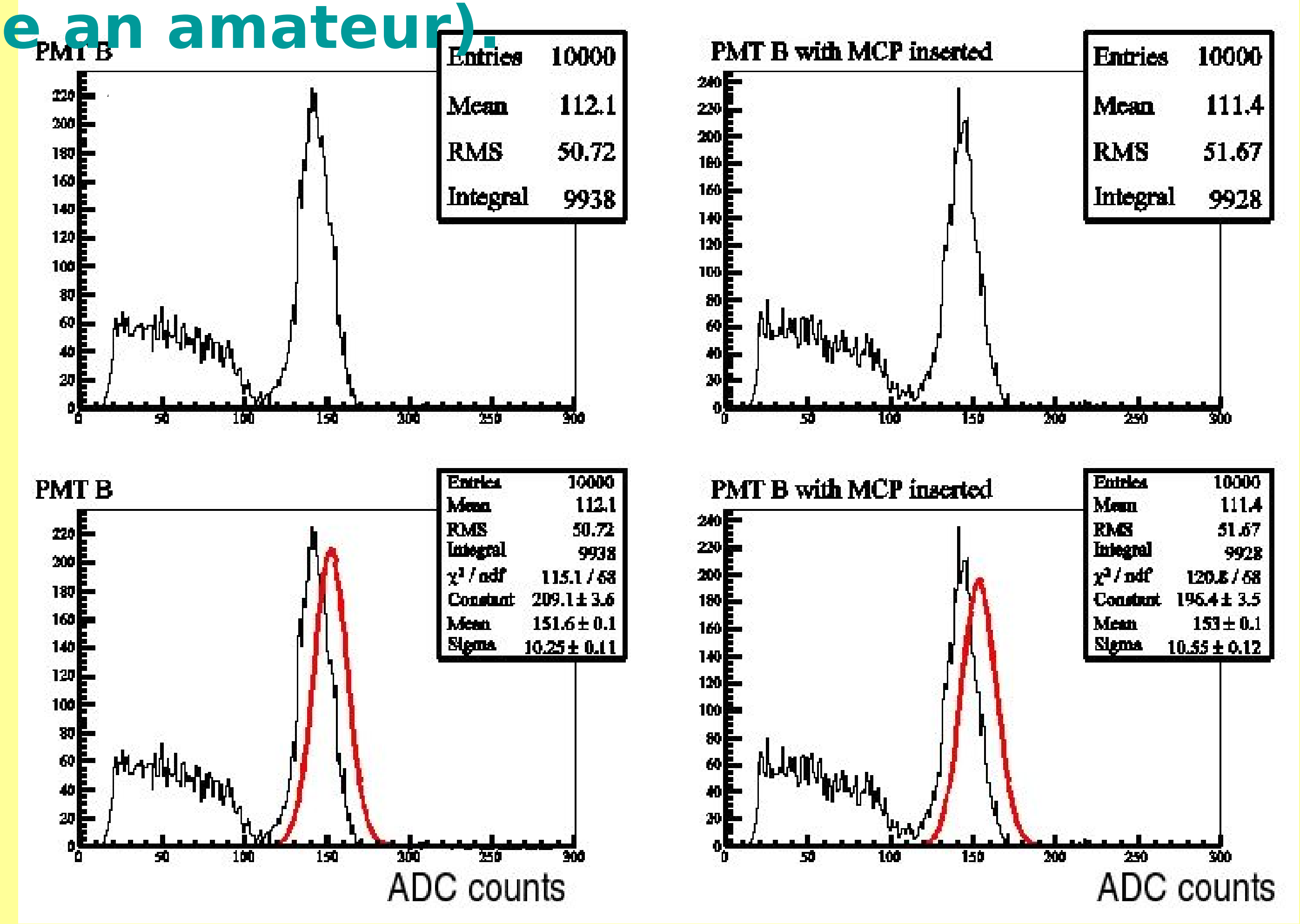
- Example- DUSEL detector with 100% coverage and 3D photon vertex reconstruction (40 cm vs res). Need 10,000 m^2 (!) (but 100M$ budget…)

Application 5- Medical Imaging (PET)



Application 5- Medical Imaging (PET)

Heejong Kim does a test: put a Planicon ahead of Bill Moses's crystal. (nice illustration of why it's nice to be an amateur).



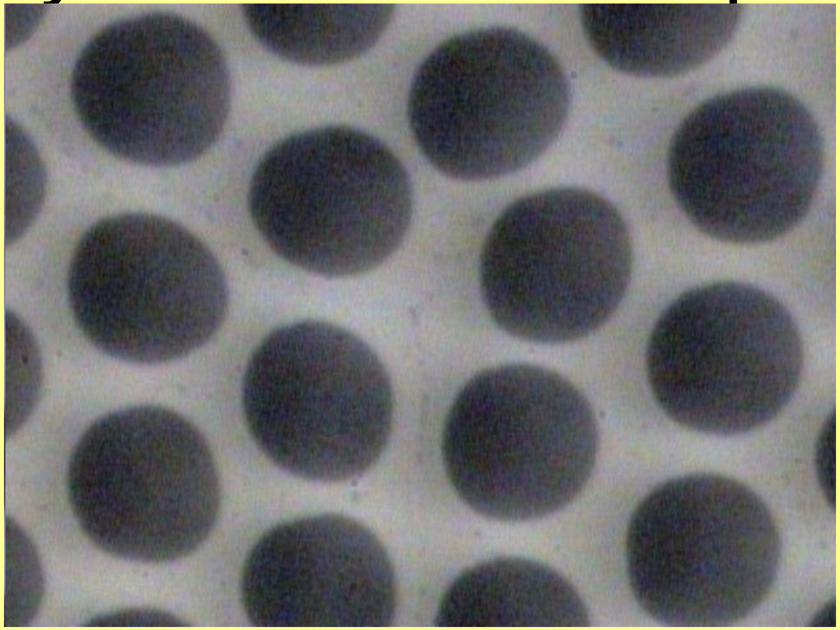
Design Goals

Colliders: ~ 1 psec resolution, < 100K$/m^2$

Neutrino H2O: ~100 psec resolution, < 10K$/m^2$

PET: ~ 30 psec resolution, < 20% of crystal cost

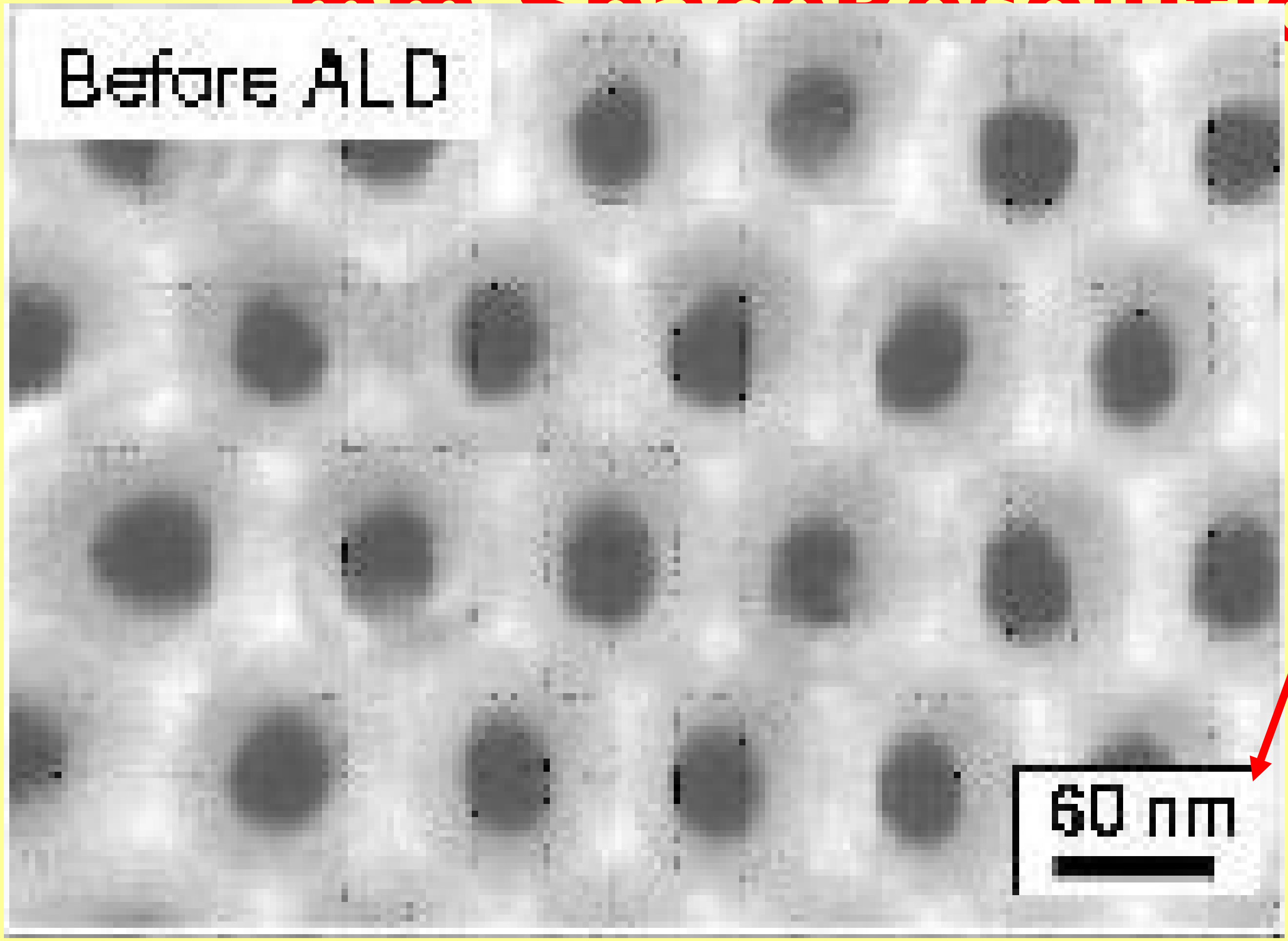
(but crystal cost not independent of readout!)



Photonis 25 micron tube- ~2M$/m^2$- not including readout- if did only what we've done so far (5cm by 5cm).

Can we make a similar structure with a batch process- e.g. AAO and ALD?

GOAL: to Develop Large-Area Photo-detectors with Psec Time and mm SpaceResolution



Too small- can go larger-

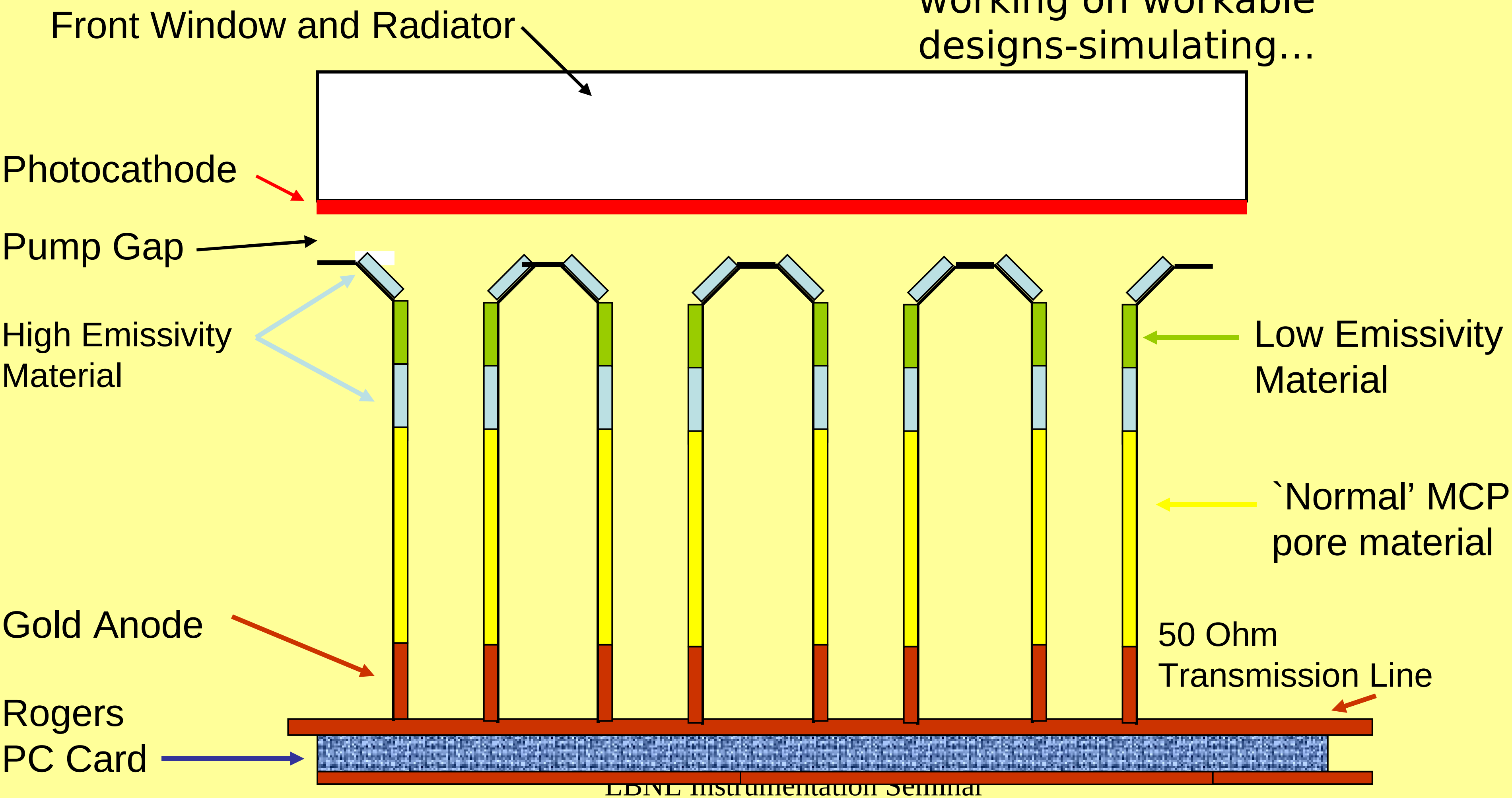
(But how does multiplication work- field lines?)

From Argonne MSD ALD web page- can we make cheap (relatively) ultra-fast planar photo-detector modules?

Psec Large-area Micro-Channel Detector

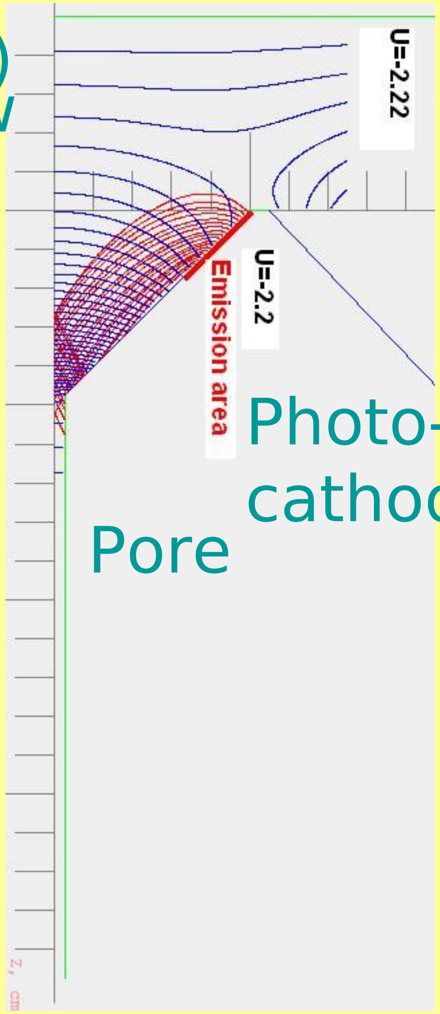
(with Hau Wang, Zeke Insepov, Mike Pellin (ANL), Valentin Ivanov (Muons.Inc), Jean-Francois Genat (UC), and others)

N.B.- this is a `cartoon'- working on workable designs-simulating…



Psec Large-area Micro-Channel Detector

(with Hau Wang, Zeke Insepov, Mike Pellin (ANL), Valentin Ivanov (Muons.Inc), Jean-Francois Genat (UC), and others)



Example of Valentin's 3D simulation program- `funnel' pore with photo-cathode on surface; blue lines are equi-potentials and red are electron trajectories.

Just started this- we're working on getting realistic inputs into the simulation. (geometry and material properties).

Also want to simulate existing Planicons to validate simulation.

Modus Operandi so far:

- In Nov. 2005, we had our 1st workshop- idea was to invite folks working or interested in related subjects- didn't know many (most) of them-
- Have developed tools and knowledge- also contact with pioneers and practictioners (Hink, Ohshima, Howorth, Va'vra,…; Breton, Delanges, Ritt, Varner)
- Development clearly too big for one group- devices, electronics, applications- have worked collaboratively with each other, national labs (Argonne, Fermilab, SLAC) and industry (Burle/Photonis, Photek, IBM,…)
- Hope is that we can continue in this style, pulling in expertise until we have the generic R&D done- then many specific applications can go separate ways.
- Yes we can (?)

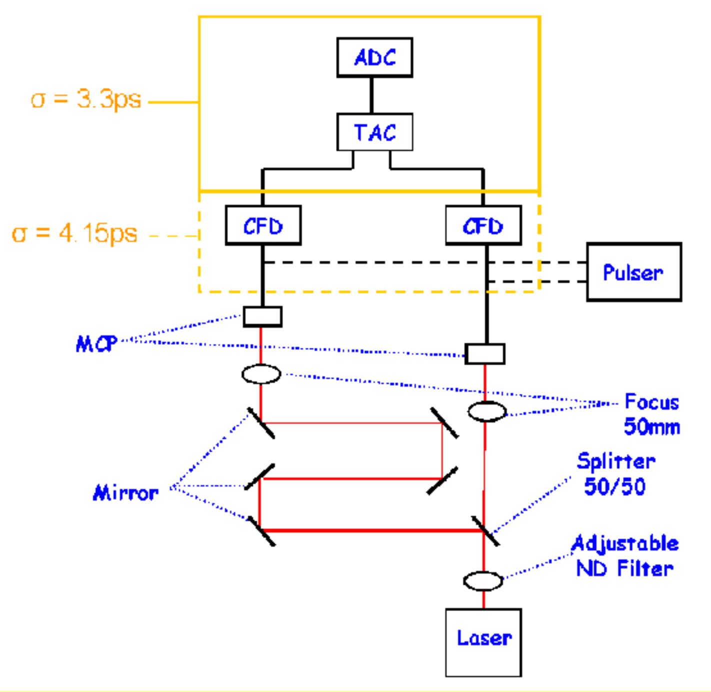
Summary- Status

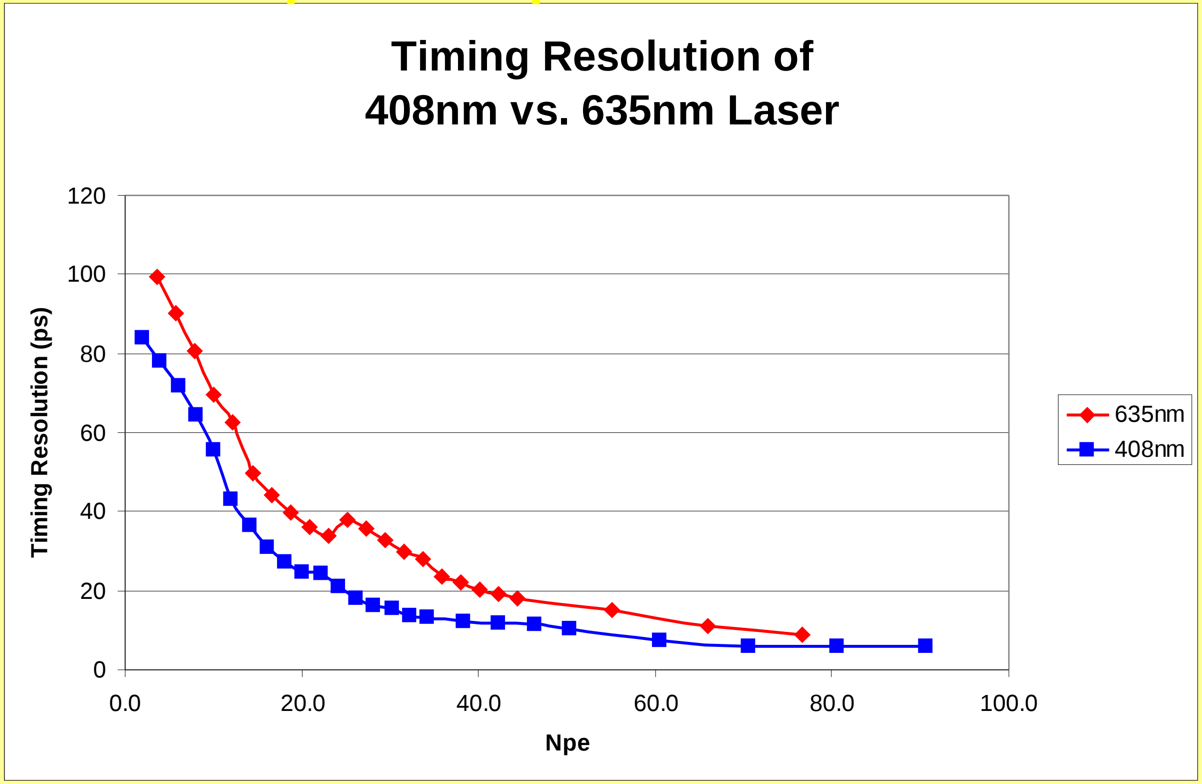
- Have good test facilities now- fast scope ($$), ANL laser test-stand, FNAL testbeam
- Have built and tested transmission line anodes; compare well with simulations.
- Have Stefan’s DRS4 chips and will have Gary’s; have IBM/CERN design kit and have been simulating in 0.13 micron; collaborating with Hawaii, Orsay; advice from PSI.
- Have started a serious effort at ANL on AAO/ALD
- Have started a serious effort at ANL/Muons.Inc on MCP device simulation.
- Think we are at the point that a 5-year 2M$/year effort has a good chance of making commercializable devices.

Thank you

Argonne Laser Lab

- Measure Δt between 2 MCP's (i.e root2 times σ); no corr for elect.
- Results: 408nm
  - 7.5ps at ~50 photoelectrons
- Results: 635nm
  - 18.3ps at ~50 photoelectrons

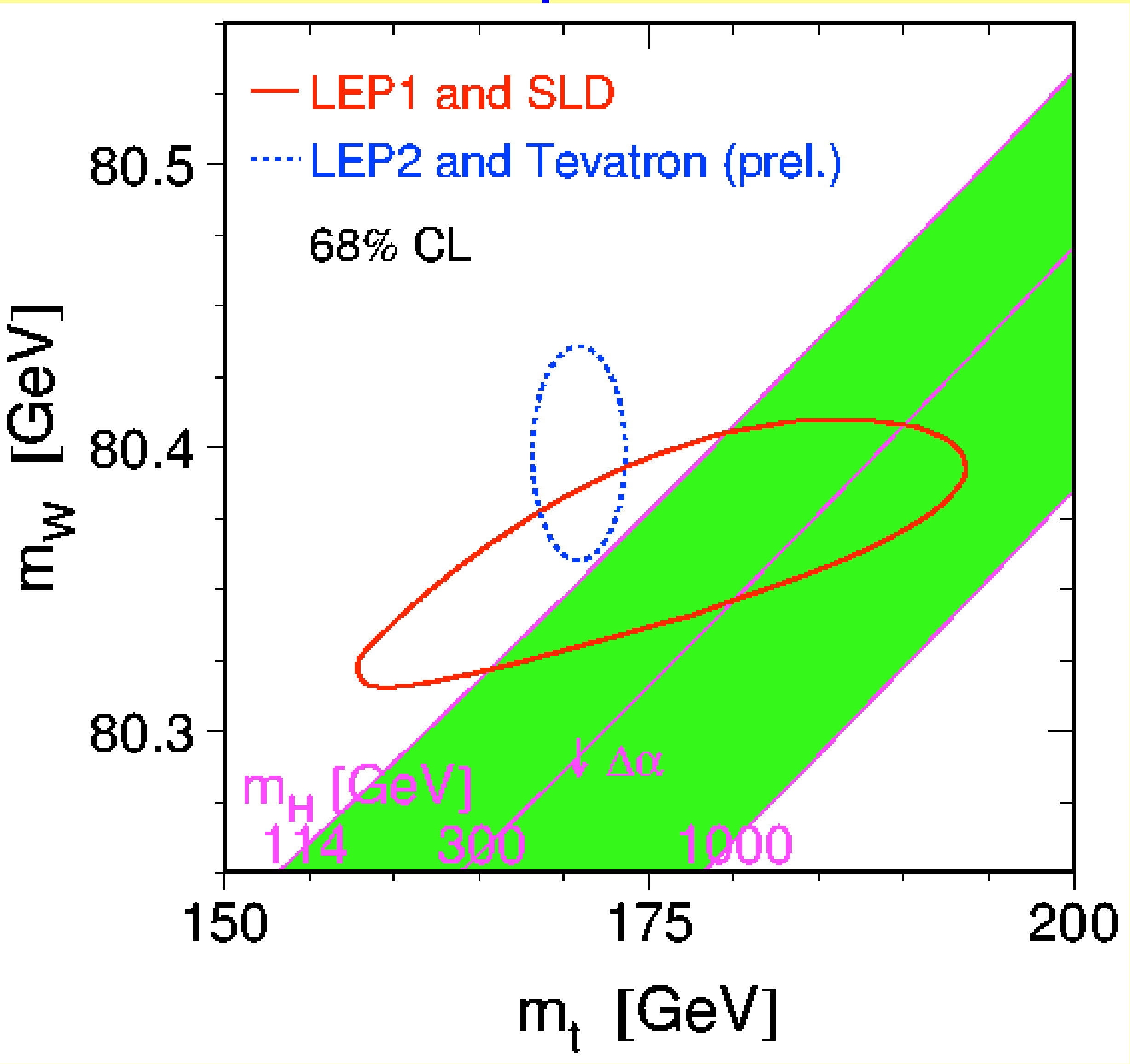




Work in Progress

- **Our way of proceding- use laser test-stand for development, validation of simulation- then move to testbeam for comparison with simulation with beam.**
  - **Changes to electronics readout**
    - **Add Ritt and/or Varner sampling readouts (interleave 10 GS) –in works**
    - **First test via SMA; then integrate chips onto boards?**
    - **Development of 40 GS CMOS sampling in IBM 8RF (0.13micron)- proposal in draft (ANL, Chicago, Hawaii, Orsay, Saclay)**
  - **Changes to the MCPs**
    - **10um pore MCPs (two in hand)**
    - **Transmission-line anodes (low inductance- matched)- in hand**
    - **Reduced cathode-MCP_IN MCP_OUT-anode gaps- ordered**
    - **ALD module with integrated anode and capacitive**

MW-Mtop Plane



M_W= 80.398 \pm 0.025 GeV (inc. new CDF 200pb^{-1})

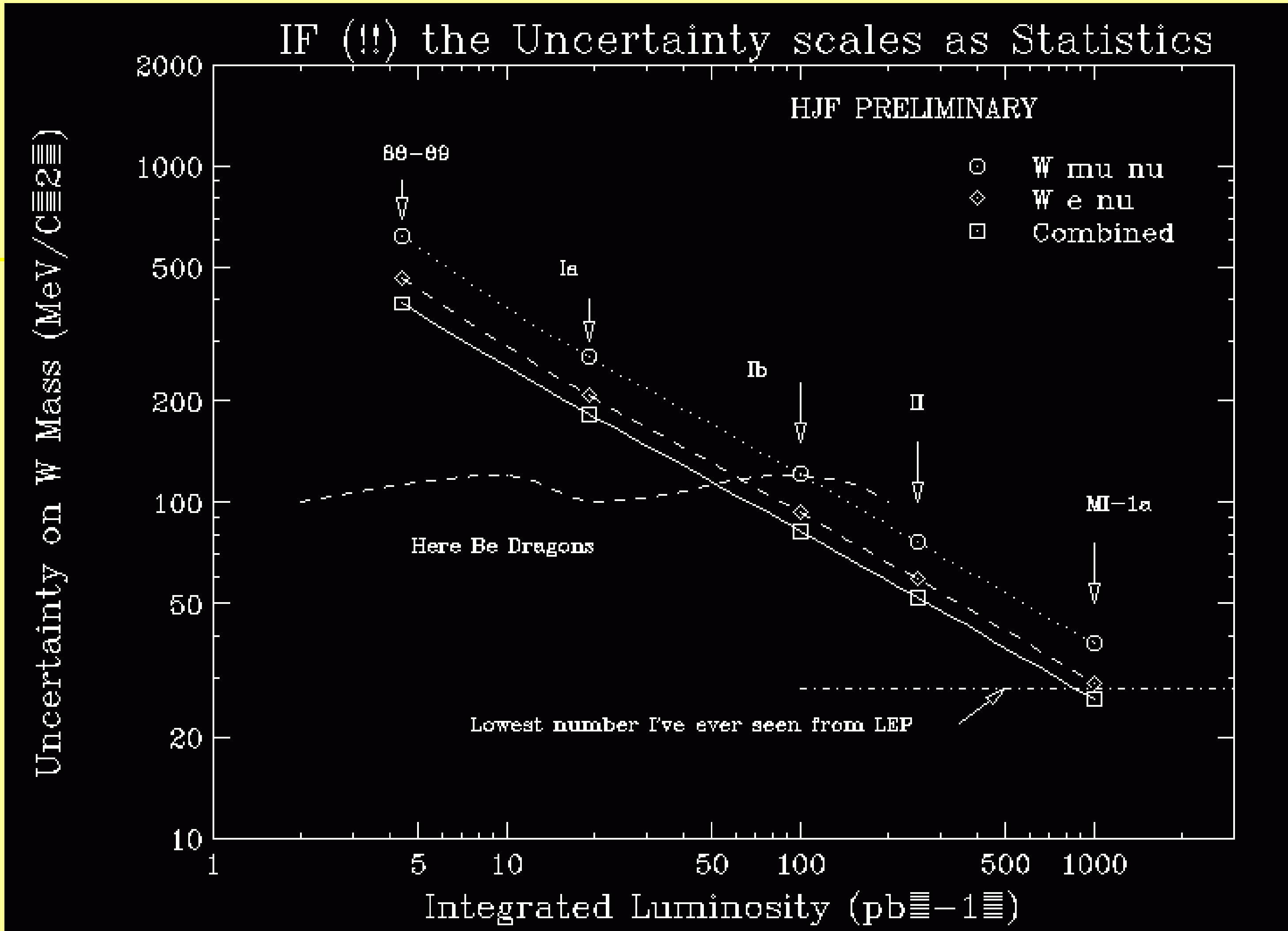
M_{top} = 170.9 \pm 1.8 GeV (March 2007)

Application 1- Collider Detector Upgrades

Take a systematics-dominated measurement: e.g. the W mass$$,

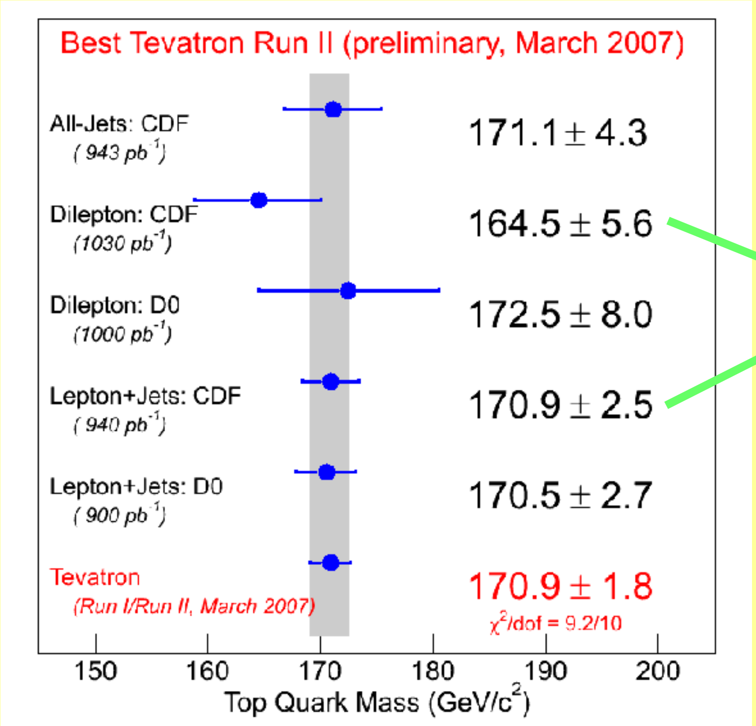
Dec 1994 (12 yrs ago)-

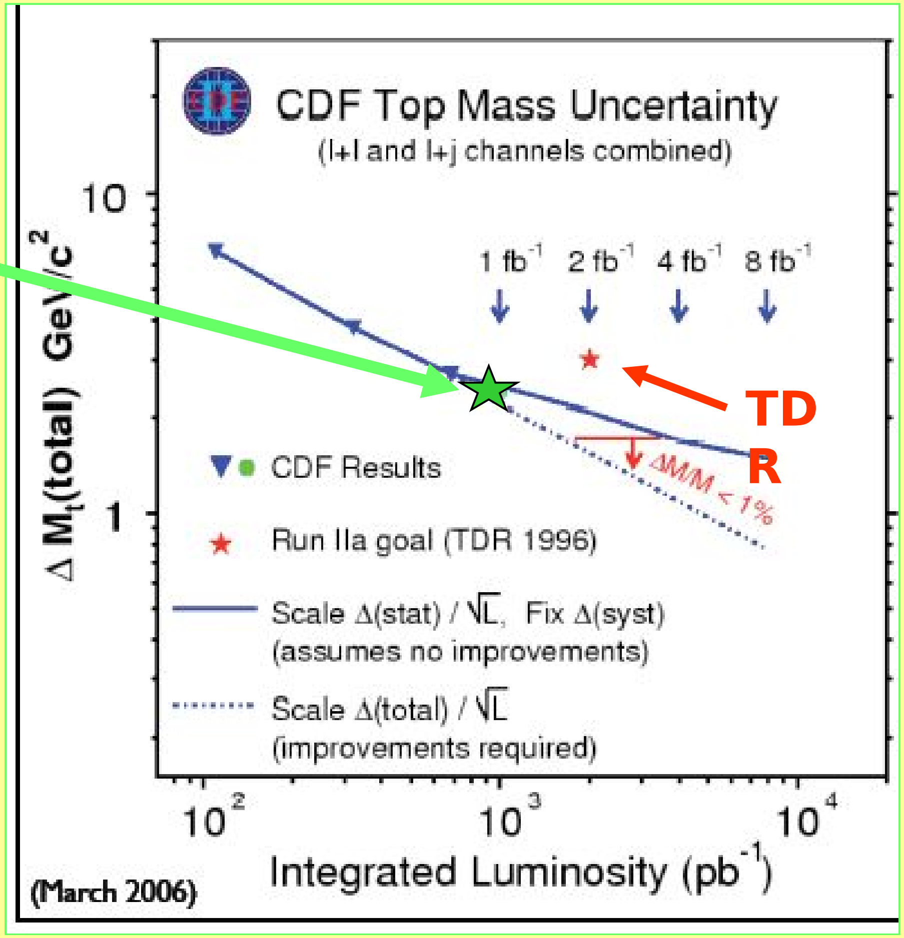
`Here Be Dragons' Slide: remarkable how precise one can do at the Tevatron (MW,Mtop, Bs mixing, …)- but has taken a long time- like any other precision measurements requires a learning process of techniques, details, detector upgrades….



Theorists too(SM)

Precision Measurement of the Top Mass





Aspen Conference Annual Values (Doug Glenzinski Summary Talk)

Jan-05: ΔMt = +/- 4.3 GeV

Jan-06: ΔMt = +/- 2.9 GeV

Jan-07: ΔMt = +/- 2.1 GeV

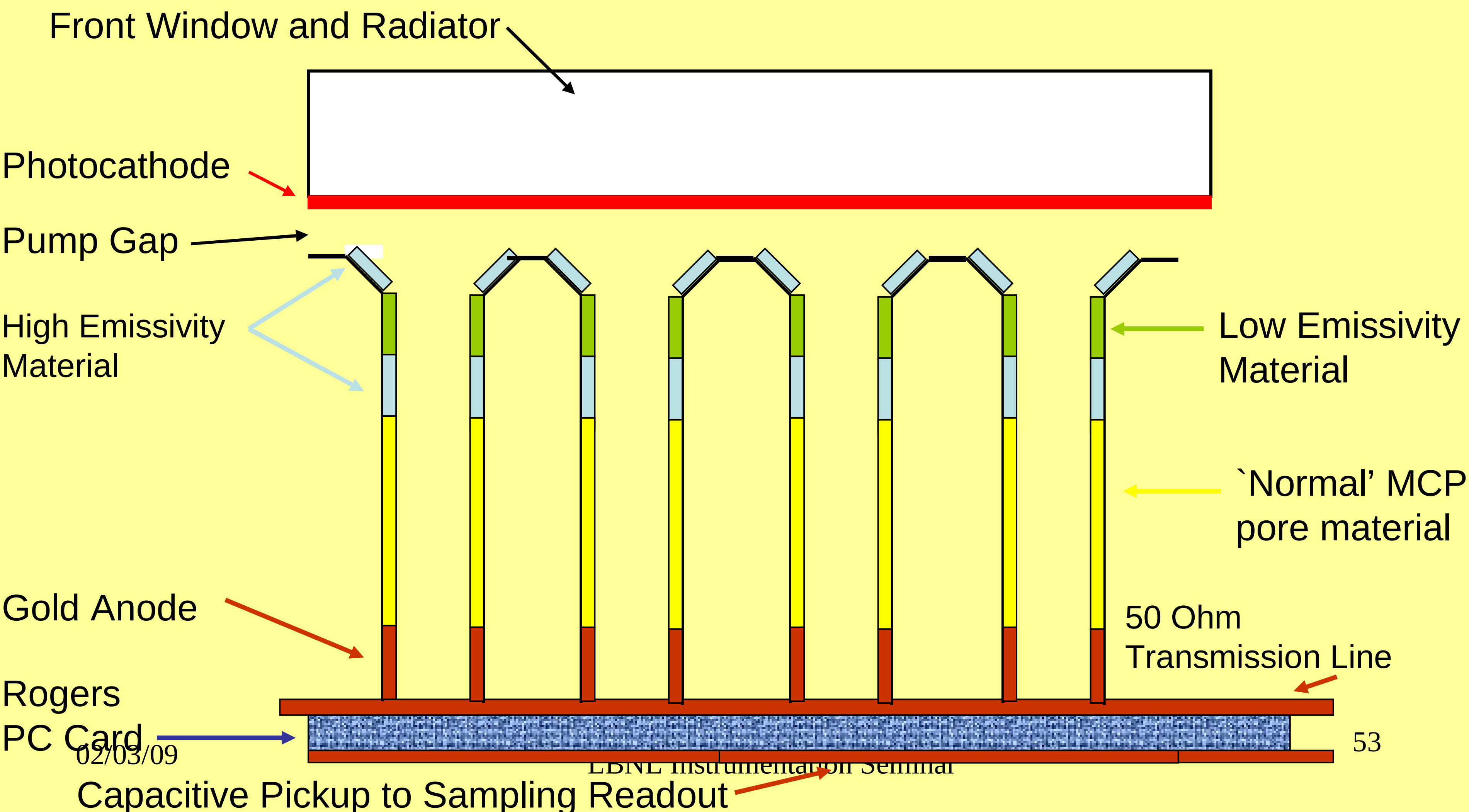
Note we are doing almost 1/root-L even now

Setting JES with MW puts us significantly ahead of the projection based on Run I in the Technical Design Report (TDR). Systematics are measurable with more data (at some level- but W and Z are

Real Possibility

- No SM Higgs is seen at the LHC
- The M-top/M-W plane says the Higgs is light.
- Serious contradiction inside the SM- `smoking gun’ for something really new…
- It will be critical to measure M_W and M-top with different systematics…

Psec Large-area Micro-Channel Plate Panel (MCPP)- LDRD proposal to ANL (with Mike Pellin/MSD)



II STATE OF THE ART

Several circuits have already been designed in the HEP community for fast pulse sampling, mainly to record photo-multipliers pulse shapes. As detailed in section I, fast timing requires higher sampling rates, but smaller dynamics ranges.

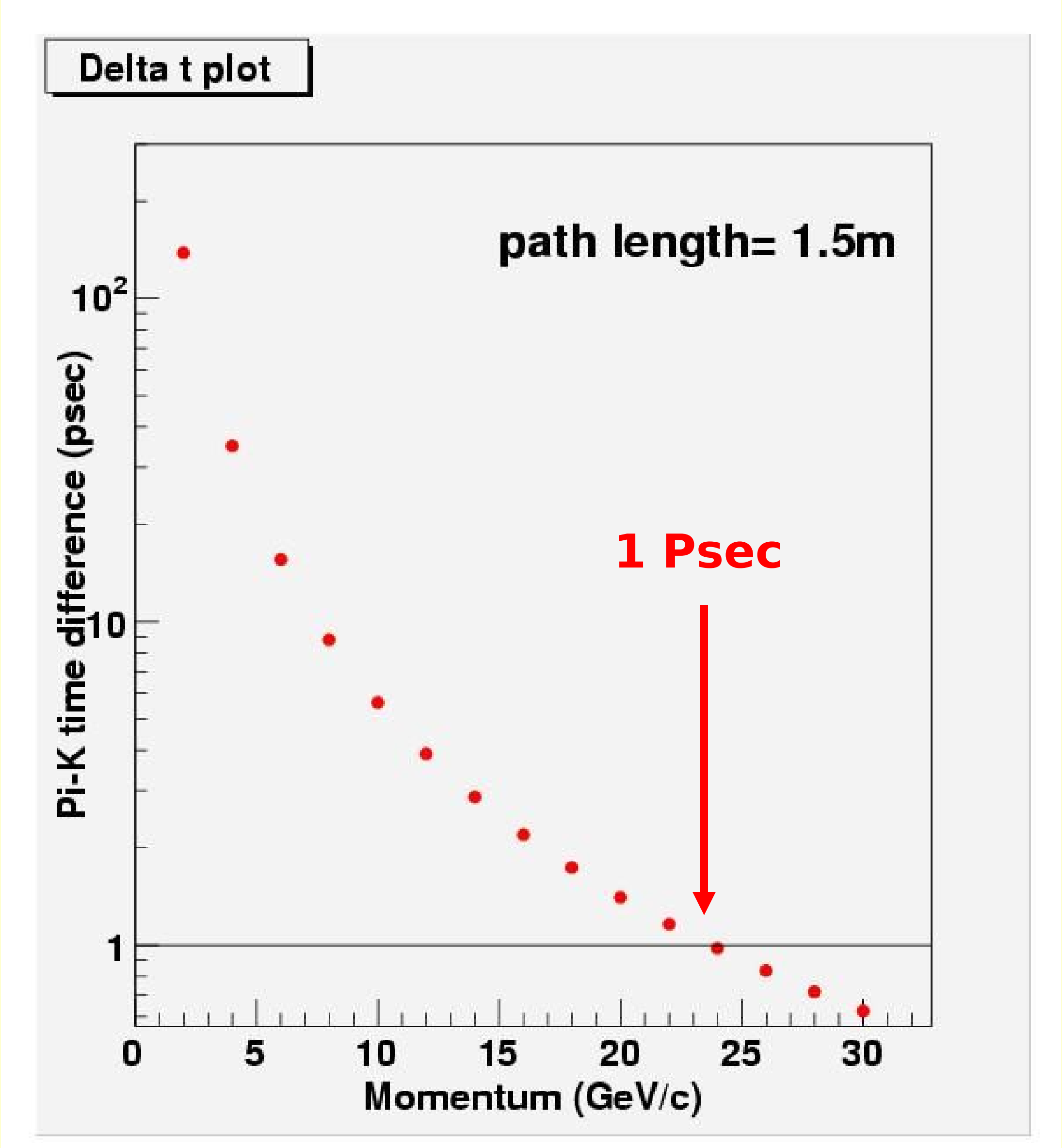
	Hawaii		Orsay/Saclay		PSI		PSEC
	Lab 3	Planned Blab2	Sam	Planned	DRS3	Planned DRS4	This proposal
Sampling frequency	20 MHz-3.7 GHz	1-10 GHz	0.7-2.5 GHz	10 GHz	10 MHz-5 GHz	5 GHz	40 GHz
Analog bandwidth	900 MHz	850 MHz	300 MHz	650 MHz	450 MHz	> DRS3	>1 GHz
Number of Channels	9	16	2		12/6/2/1	8/4/2/1	16
Triggered mode	Common Stop	Channel trigger on sums	Common Stop		Common Stop	Common Stop	Channel trigger
Resolution		10 bit	11.6 bit		11.6 bit	11.5 bit	8-10 bit
Samples	256	4/8 rows of 512	256	2048	1024-12288	1024-8192	64
Clock	33 MHz	33 MHz	66 MHz		20 MHz	fsamp/2048	60 MHz
Max latency			5ms		0.6 ms		
Input Buffers		TIA (5kOhm gain)	Yes	No	No	No	Yes
Differential Inputs	No	Pseudo-diff	Yes		Yes	Yes	Pseudo diff
Input impedance	50 Ohms Ext	30-70Ohms adjustable	> 10 MOhm			7-11pF	
Readout clock		1 GHz Wilkinson	16 MHz		33 MHz	33 MHz	60 MHz
Readout time	150µs	512µs	< 2 µs		30ns * N samples	30ns * N samples	< 1 µs
Locked delays	Ext DAC	Ext DLL	Int DLL		Ext PLL	Int PLL	
On-chip ADC	Yes	1 GHz Wilkinson	No		No	No	Yes
R/W simultaneous		Yes	No		No	Yes	No
Power/ch	50mW	20mW/sample 0.2W/read	150 mW		1-13mW	2-20mW	
Dynamic range		1mV/1V	0.65mV-2V		0.35mV/1.1V	0.35/1V	1V
Xtalk	Average << 10%	< 0.1%	0.30%		<0.5%	<0.5%	
Sampling jitter		TBD	40ps		200ps (Ext PLL)	Ext PLL	10ps
Power supplies	2.5V	2.5V	0-3.3V		2.5V	2.5 V	1.8V
Process	TSMC 0.25	TSMC 0.25	AMS 0.35	AMS 0.18	UMC 0.25	UMC 0.25	CMOS 0.13
Chip area	2.5 mm2	12 mm2	10 mm2		25 mm2	25 mm2	1 mm2
Cost/channel		500$/40 10$/2k	15.7$/12k			10-15$	

Table 1. State of the art, this proposal. The yellow column is from Gary Varner's group at the University of Hawaii (USA) [12], the light blue from Dominique Breton from the University of Paris-Sud (Orsay) [10] and Eric Delagnes from CEA (Saclay), (France) [11]. The orange column from Stefan Ritt at PSI (Switzerland) [13]. The dark blue is this proposal.

Summary

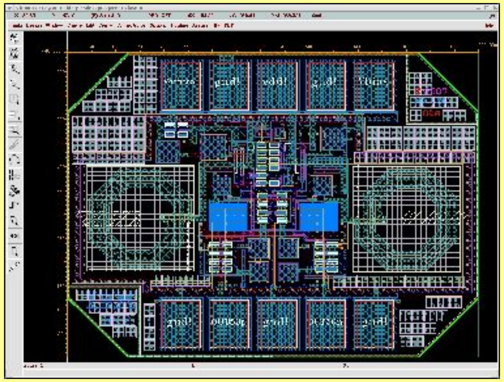
- Next step is to make anodes that give both position and time- hope is few mm and << 10 psec resolutions. This would allow systems of (say) 6” by 6” size with ~100 channels- good first step.
- Muon cooling is a nice first application of psec tof- not to big, very important, savings of money.
- We have made a number of false starts and wrong turns (e.g. the IBM bipolar 200 GHz electronics), but the fundamentals look good- don’t see a hard limit yet.

K-Pi Separation over 1.5m

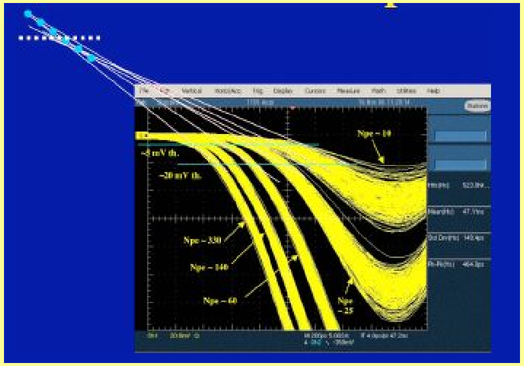


Assumes perfect momentum resolution (time res is better than momentum res!)

Engineering Highlights



- F.Tang (UChicago) designed Voltage Control Oscillator using IBM 0.13um SiGe BiCMOS8HP
- More challenging - Time Stretcher chip (including ultra low timing jitter/walk discriminator & dual-slope ramping time stretching circuits etc.)
  - From simulations, accuracy not good enough (5-10 psecs) F.Tang
  - Power concerns
- NEW: Invented 2 new schemes - a) Multi-threshold comparators, b) 50 GHz 64-channel waveform sampling. Both schemes give energy and leading edge time.
- Current plan: Save waveform and use multiple thresholds to digitize. Use CMOS (J.F. Genat, UChicago)
  - Dec meeting at UChicago with UChicago, ANL, Saclay, LBL & Hawaii, IBM and Photonis



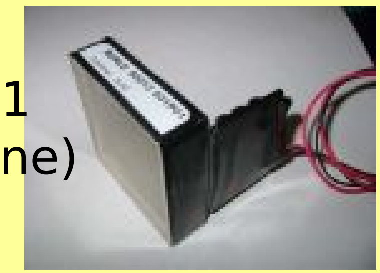
MCP Best Results

Previous Measurements:

– Jerry Va'vra SLAC (Presented at Chicago Sep 2007)

- Upper Limit on MCP-PMT resolution: $\sigma_{\text{MCP-PMT}} \sim 5$ ps

urle/Photonis MCP-PMT 85012-501
4 pixels, ground all pads except one)



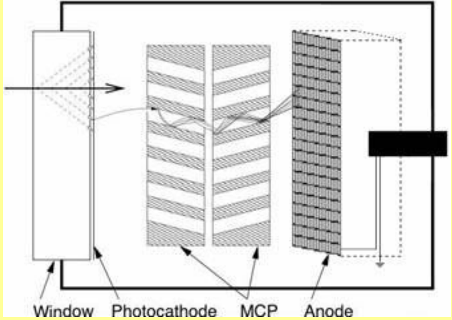
- Using two 10 um MCP hole diameter
- PiLAS red laser diode (635 nm)
- 1cm Quartz radiator (Npe ~ 50)

– Takayoshi Ohshima of University of Nagoya (Presented at SLAC Apr 2006)

- Reached a $\sigma_{\text{MCP-PMT}} \sim 6.2$ps in test beam

- Use 2 identical 6 micron TOF detectors in beam (Start & Stop)
- Beam resolution with qtz. Radiator (Npe ~ 50)

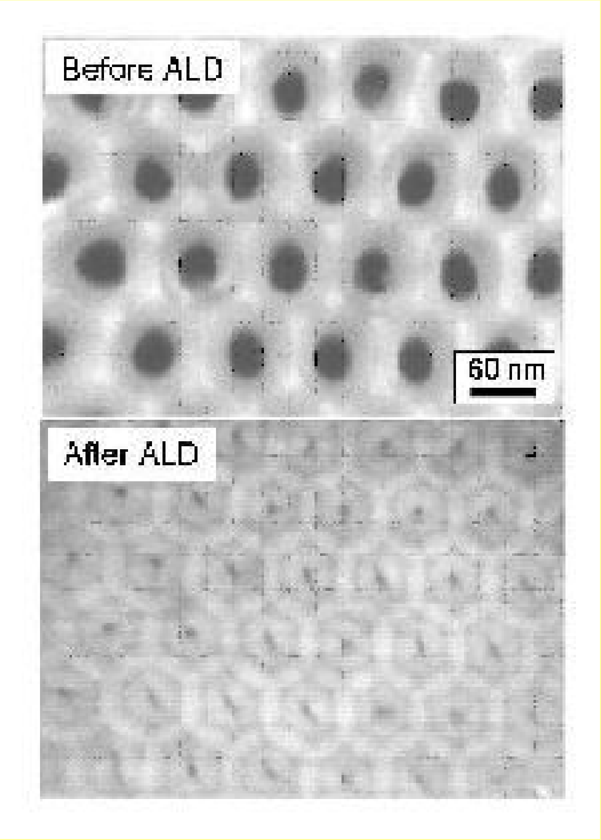
R&D of MCP-PMT Devices



We are exploring a psec-resolution TOF system using micro-channel plates (MCP's) incorporating:

- A source of light with sub-psec jitter, in this case Cherenkov light generated at the MCP face (i.e. no bounces): Different thicknesses of Quartz Radiator
- Short paths for charge drift and multiplication: Reduced gap
- A low-inductance return path for the high-frequency component of the signal:
- Optimization of the anode for charge-collection over small transverse distances:
- The development of multi-channel psec-resolution custom readout electronics directly mounted on the anode assembly: ASIC, precision clock distribution
- Smaller pore size: Atomic Layer Deposition

Atomic Layer Deposition



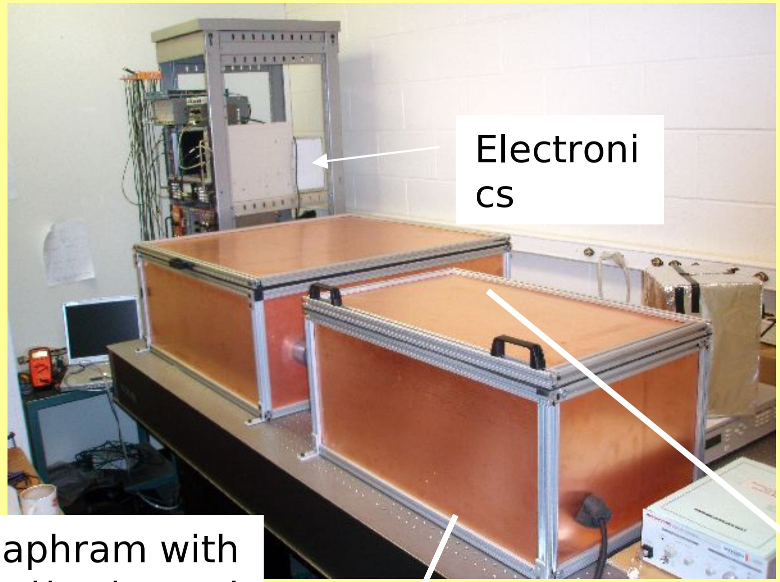
M.Pellin, MSD

- ALD is a gas phase chemical process used to create extremely thin coatings.
- **Current 10 micron MCPs have pore spacing of 10,000 nm**. Our state of the art for Photonis MCPs is 2 micron (although the square MCPs are 10 micron).
- **We have measured MCP timing resolution folk-lore is that it depends strongly on pore size, and should improve substantially with smaller pores (betcha).**

Karen Byrum slide, mostly

FY-08 Funds –ANL

Laser Test Stand at Argonne



Hamamatsu PLP-10 Laser (Controller w/a laser diode head) 405 & 635nm head.

Pulse to pulse jitter < 10psec (Manufacture Specs)