FTK: a Fast Track Trigger for ATLAS

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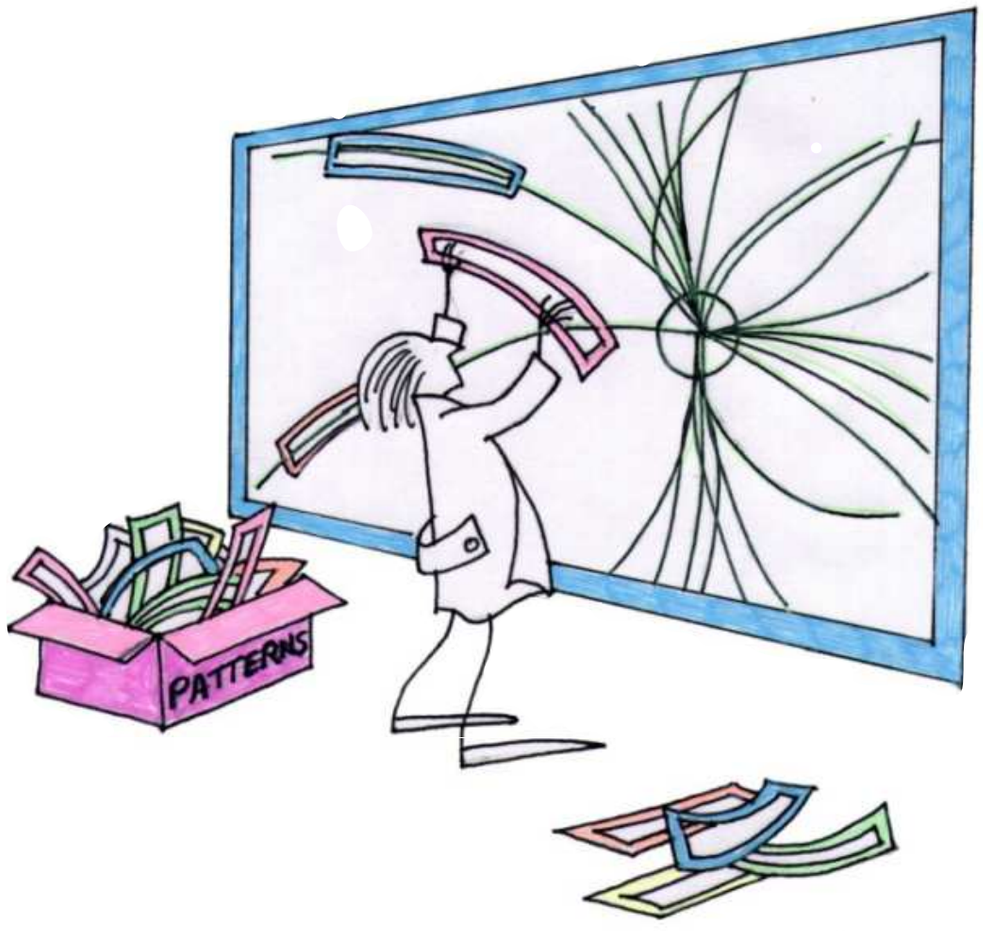
THE UNIVERSITY OF CHICAGO



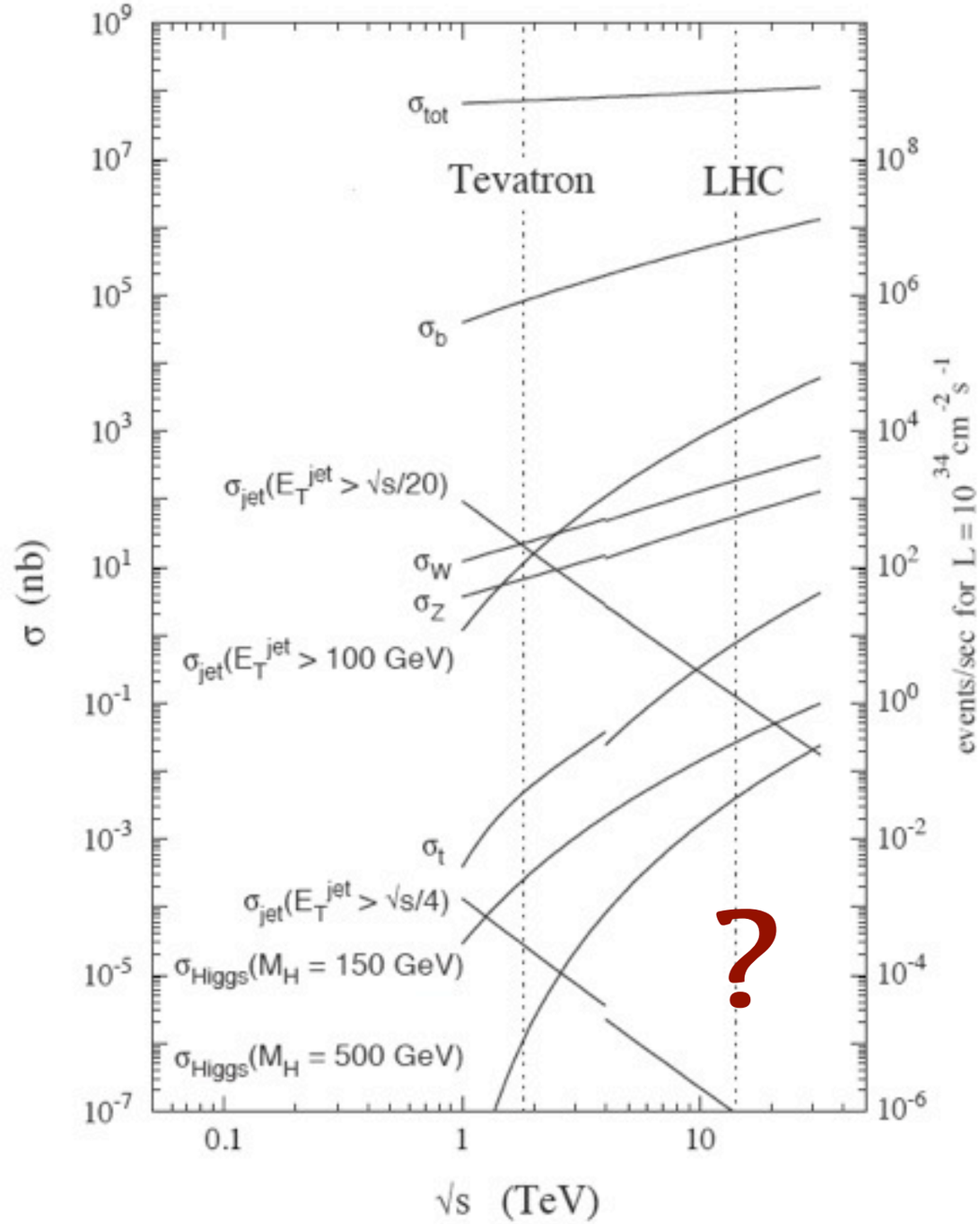
Physics goals at the Energy Frontier

- **Finding the Higgs** and figuring out what type of Higgs it is

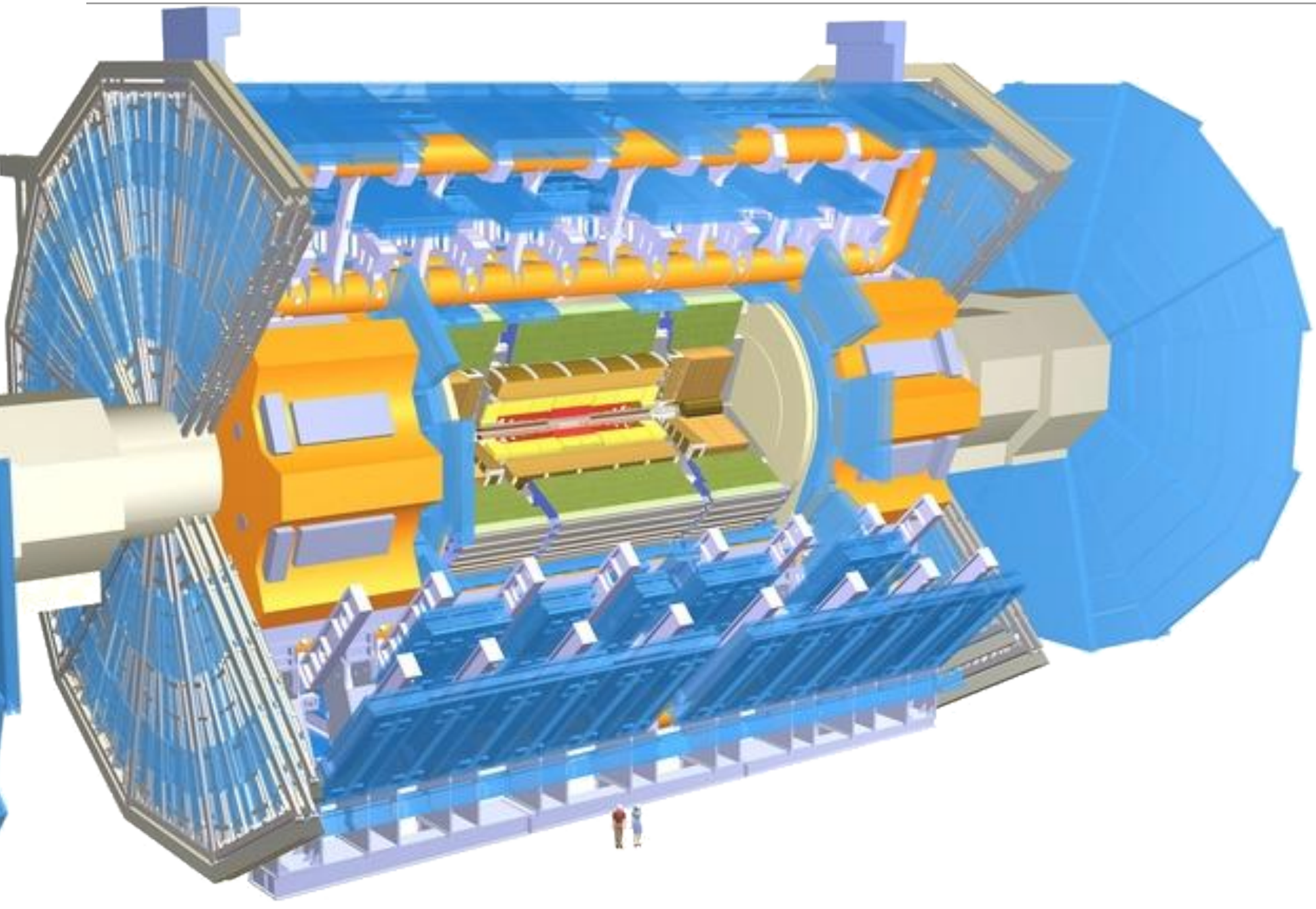
- Search for "New Physics"

- Searching for candidate dark matter particles

- **BUT**: Cross-sections are still tiny--need to be at the luminosity frontier too!



ATLAS



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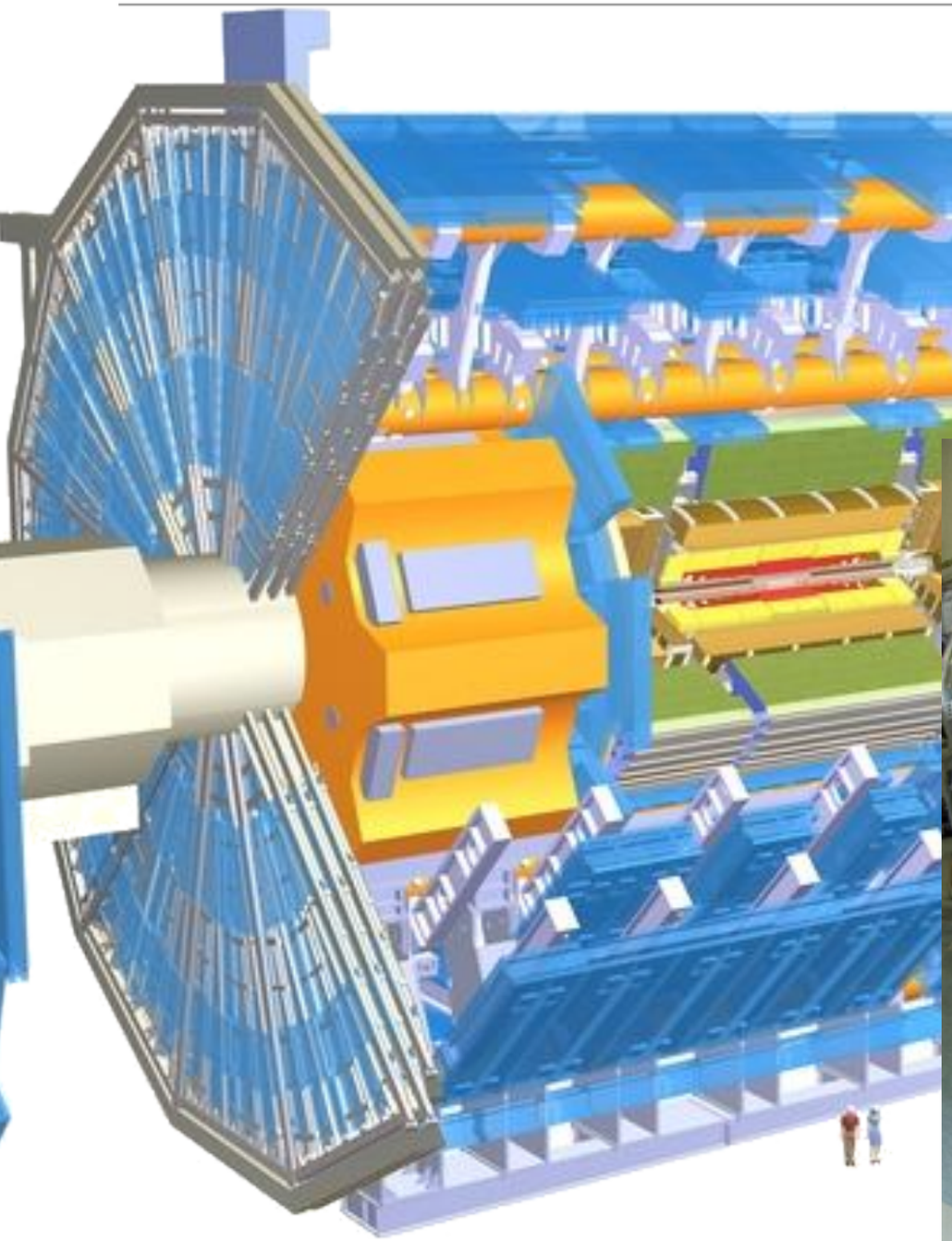

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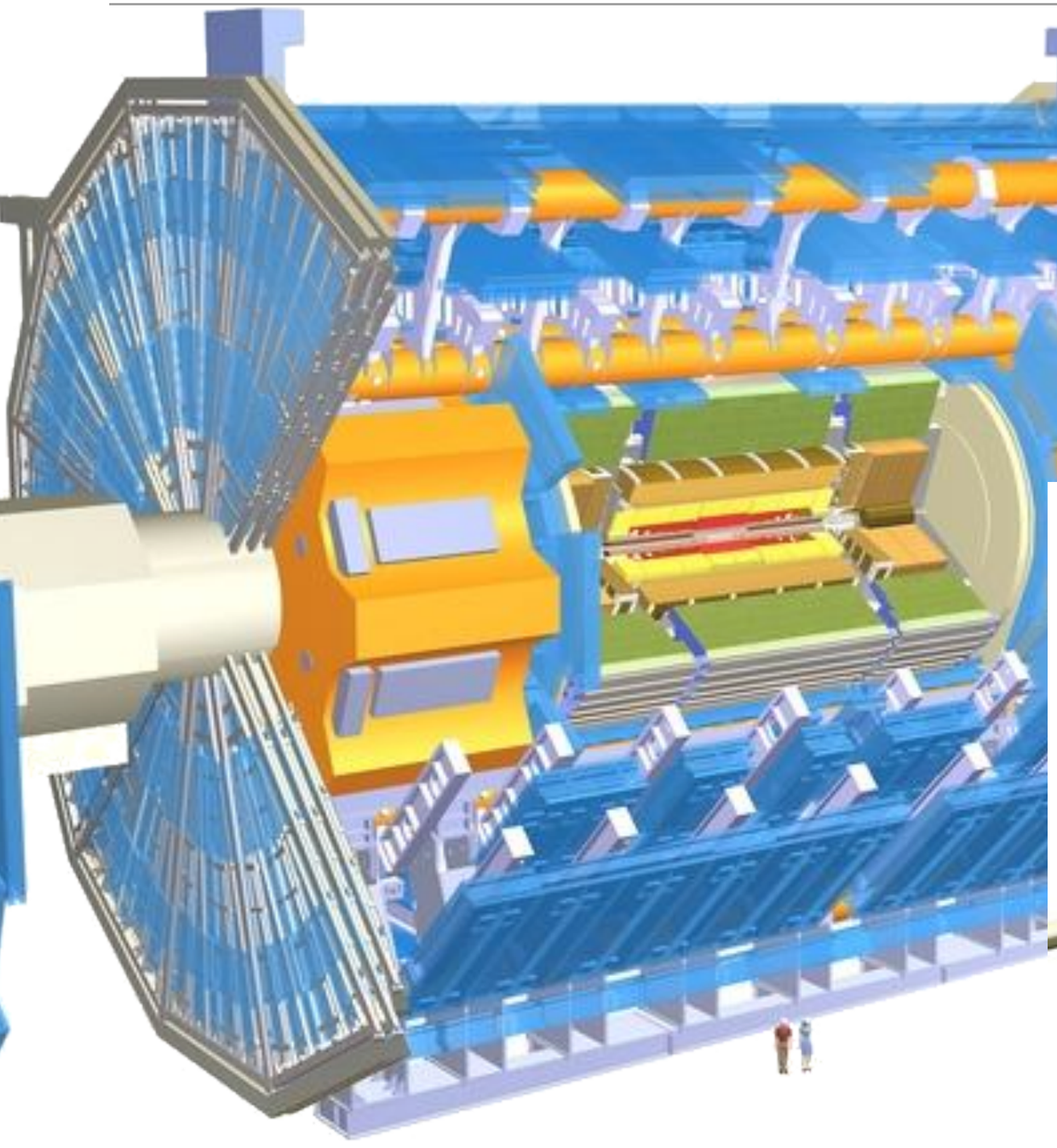
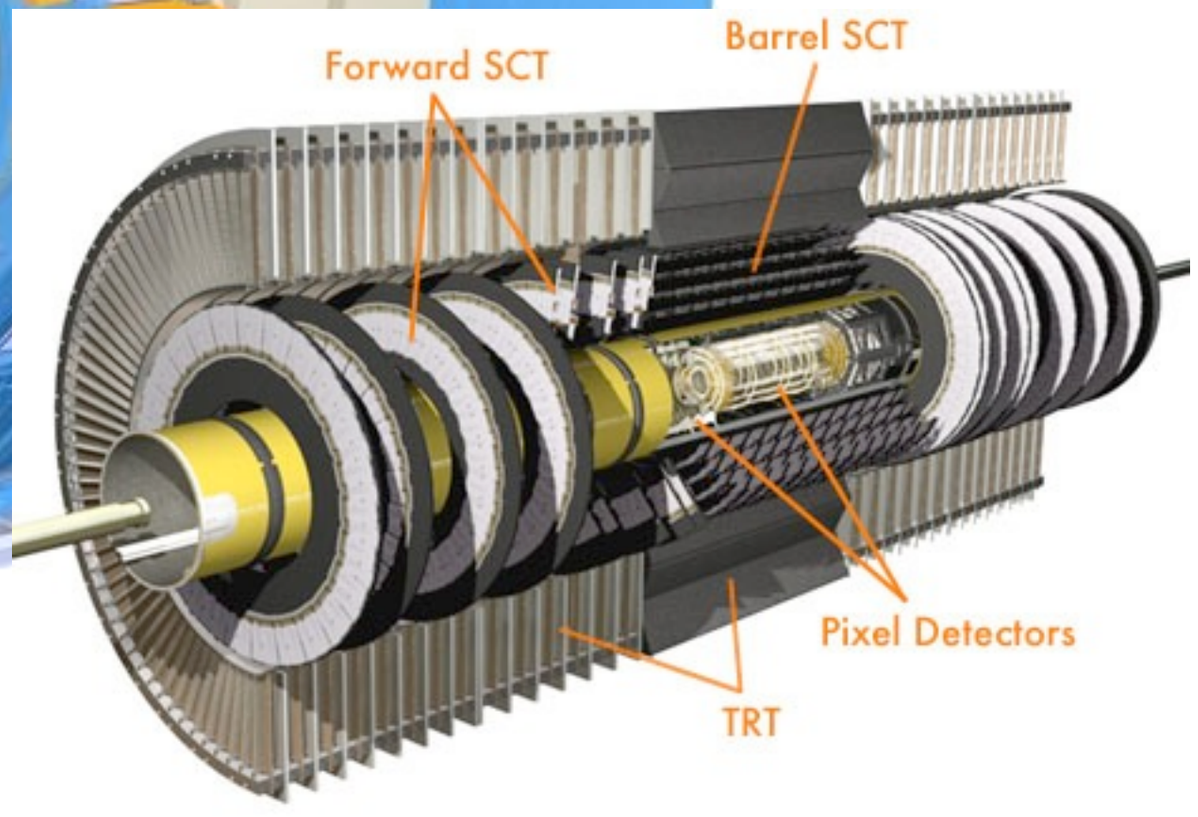
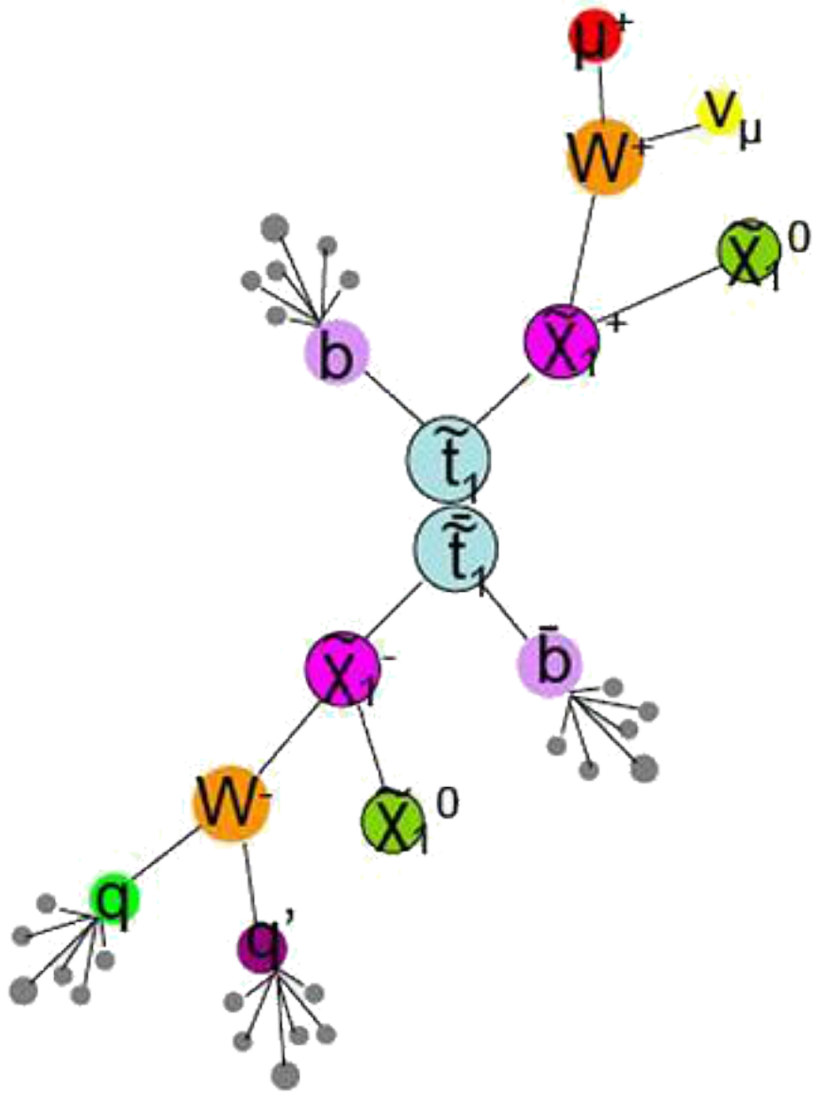


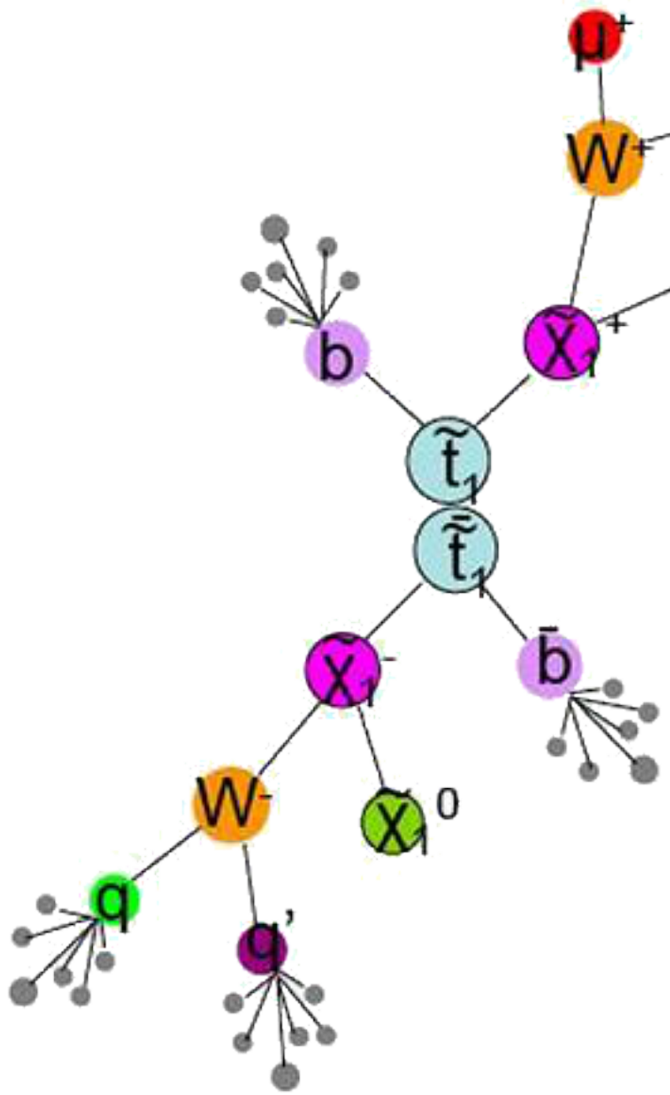


Challenges



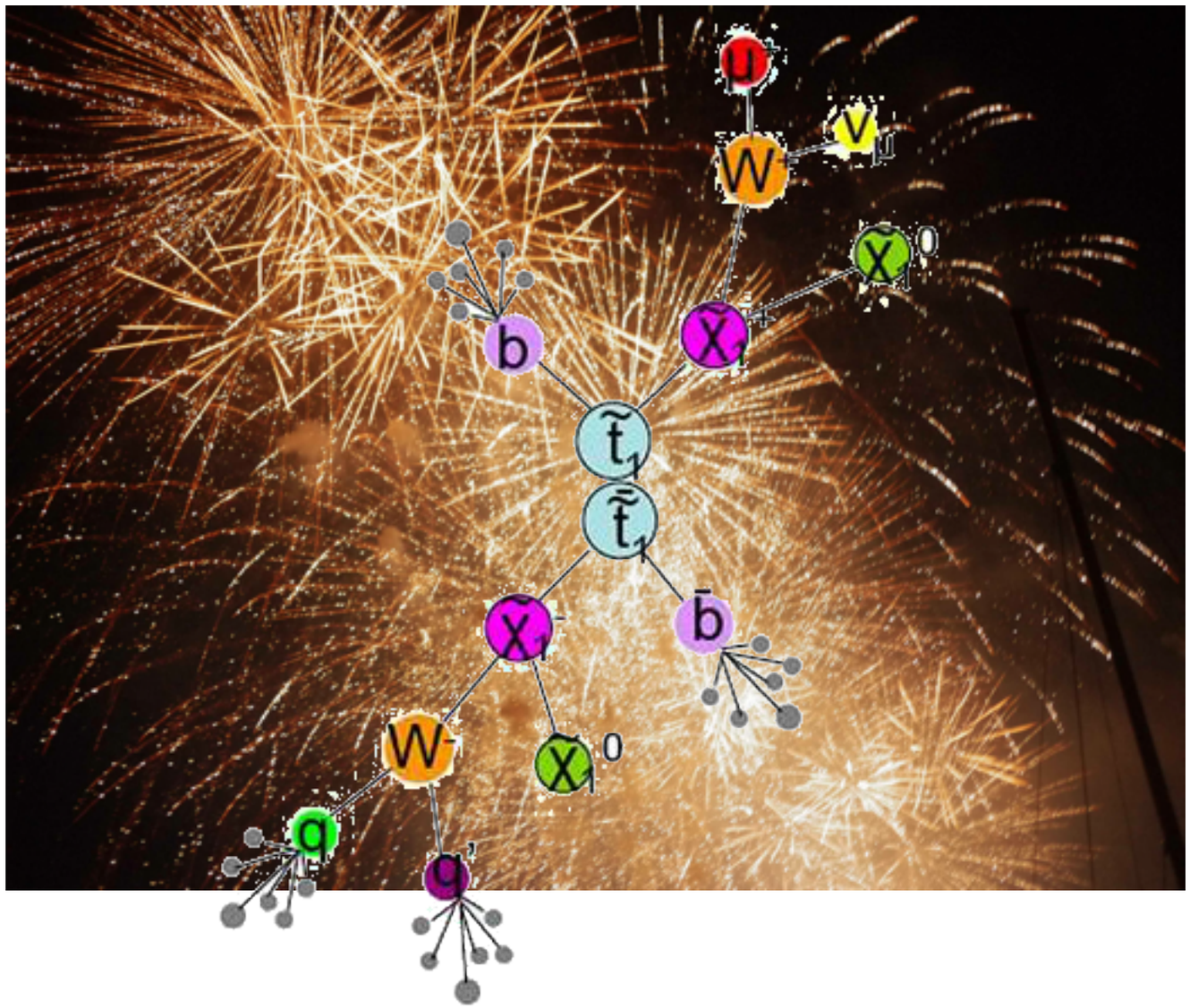
Challenges

- Need to trigger quickly and efficiently on:
  - **Leptons from electroweak decays: Isolated electrons and muons**
  - **3rd generation particles: taus, b-quarks**
  - Jets and Missing Energy

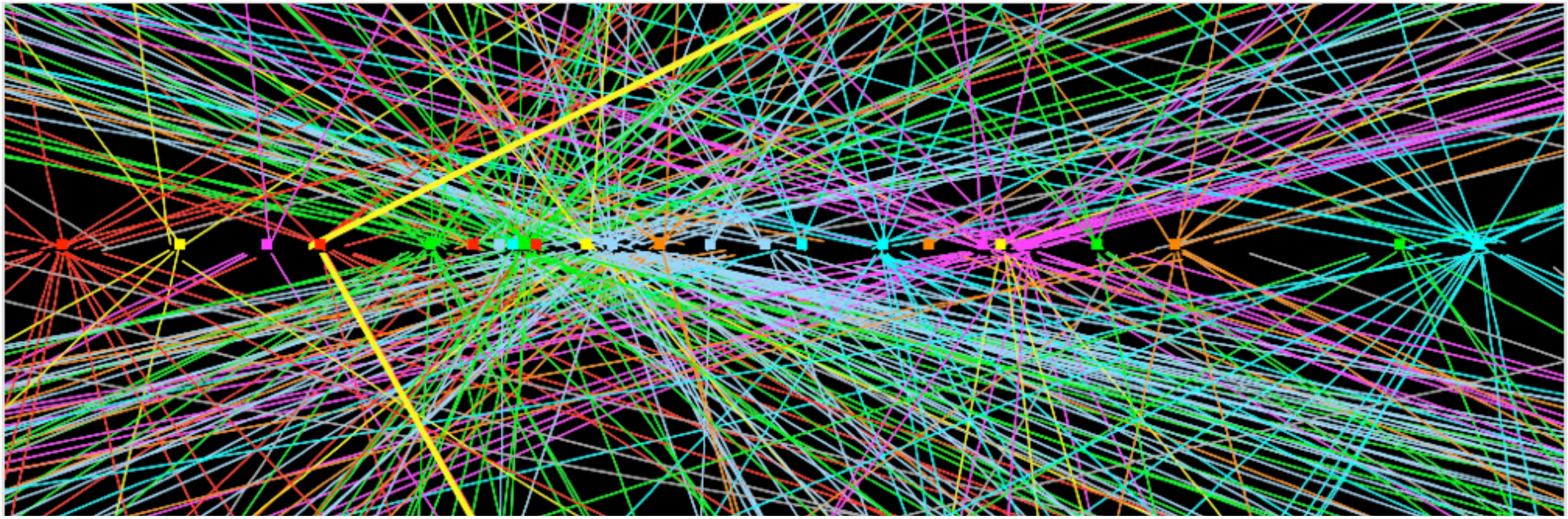


Challenges

- Need to trigger quickly and efficiently on:
  - **Leptons from electroweak decays: Isolated electrons and muons**
  - **3rd generation particles: taus, b-quarks**
  - Jets and Missing Energy
- The environment:
  - Currently: 25 interactions every 50 ns
  - Future: 70 interactions every 25 ns

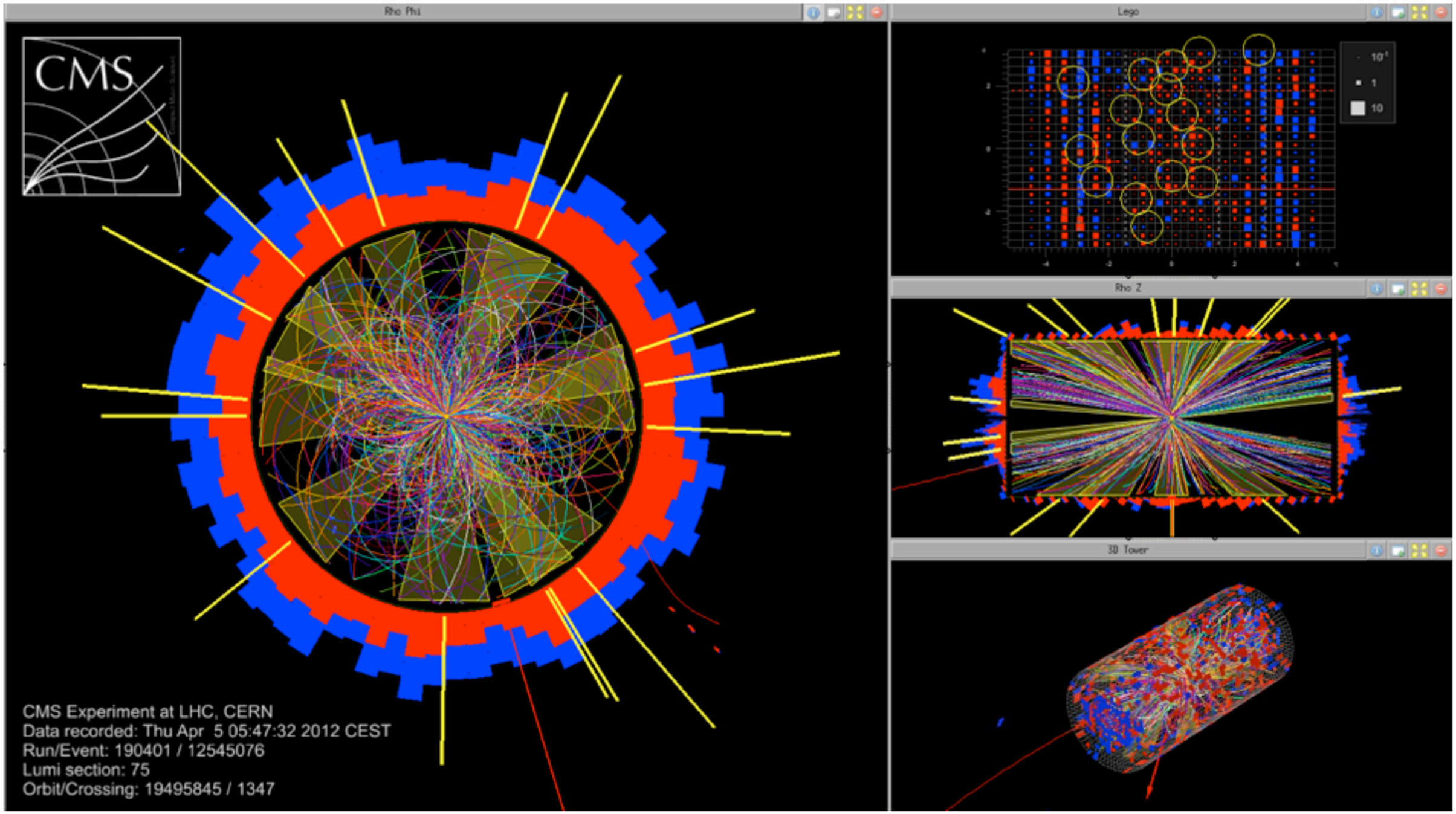


Challenges



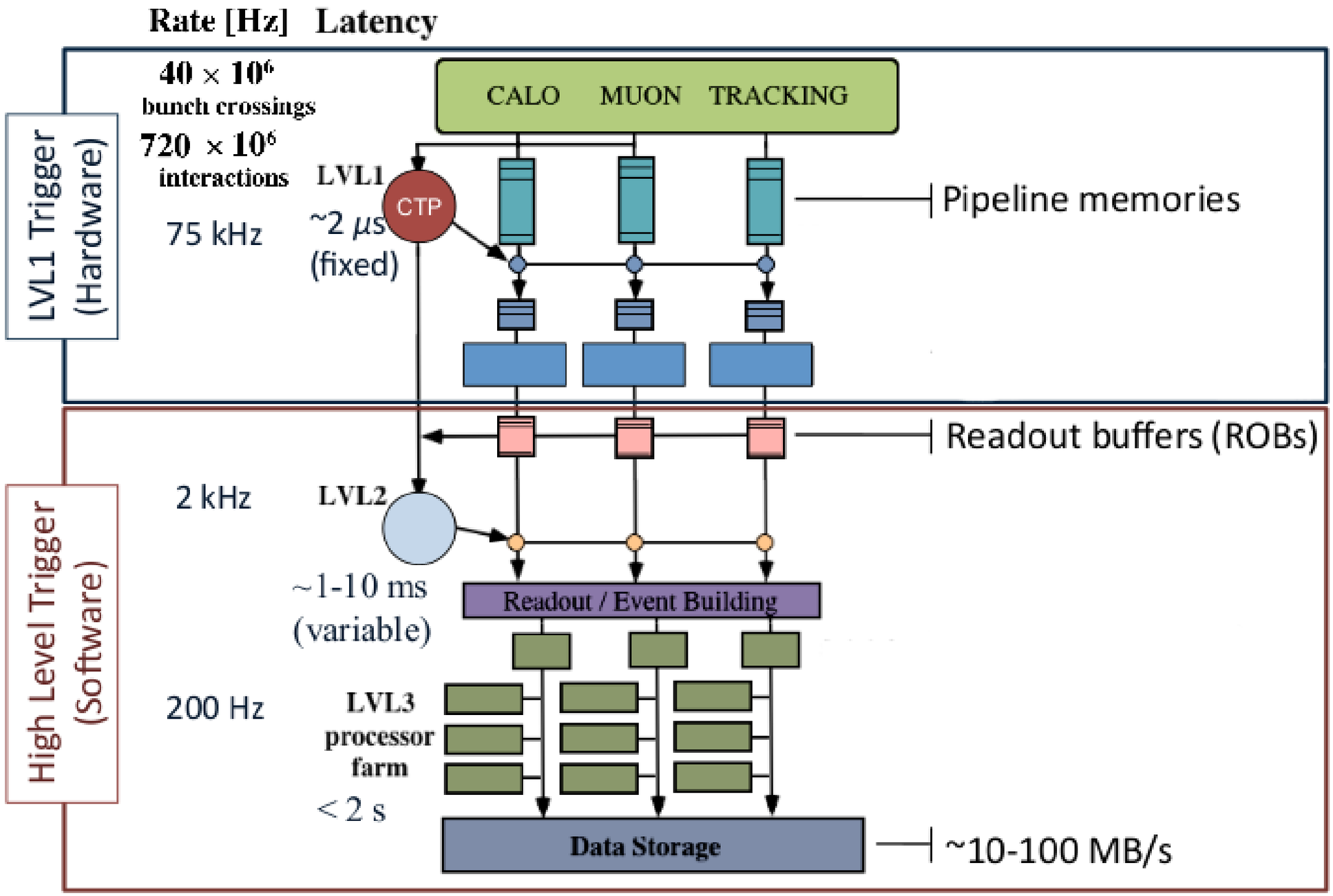
April 15th 2012, 25 reconstructed vertices, $Z \rightarrow \mu\mu$ candidate event

Challenges

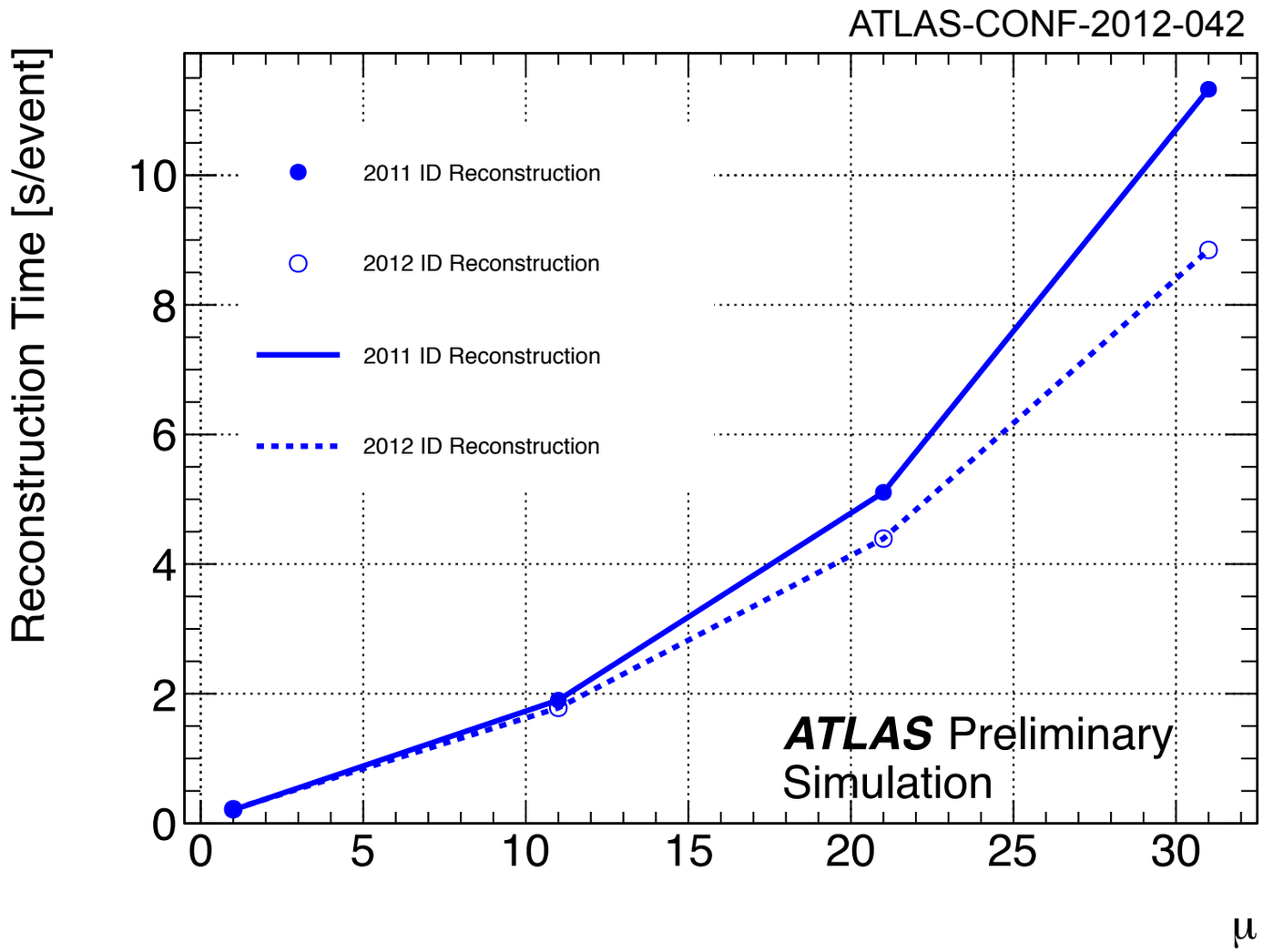


April 5th 2012, 23 (?) reconstructed vertices

ATLAS Trigger System



Tracking at High Lumi is Tricky

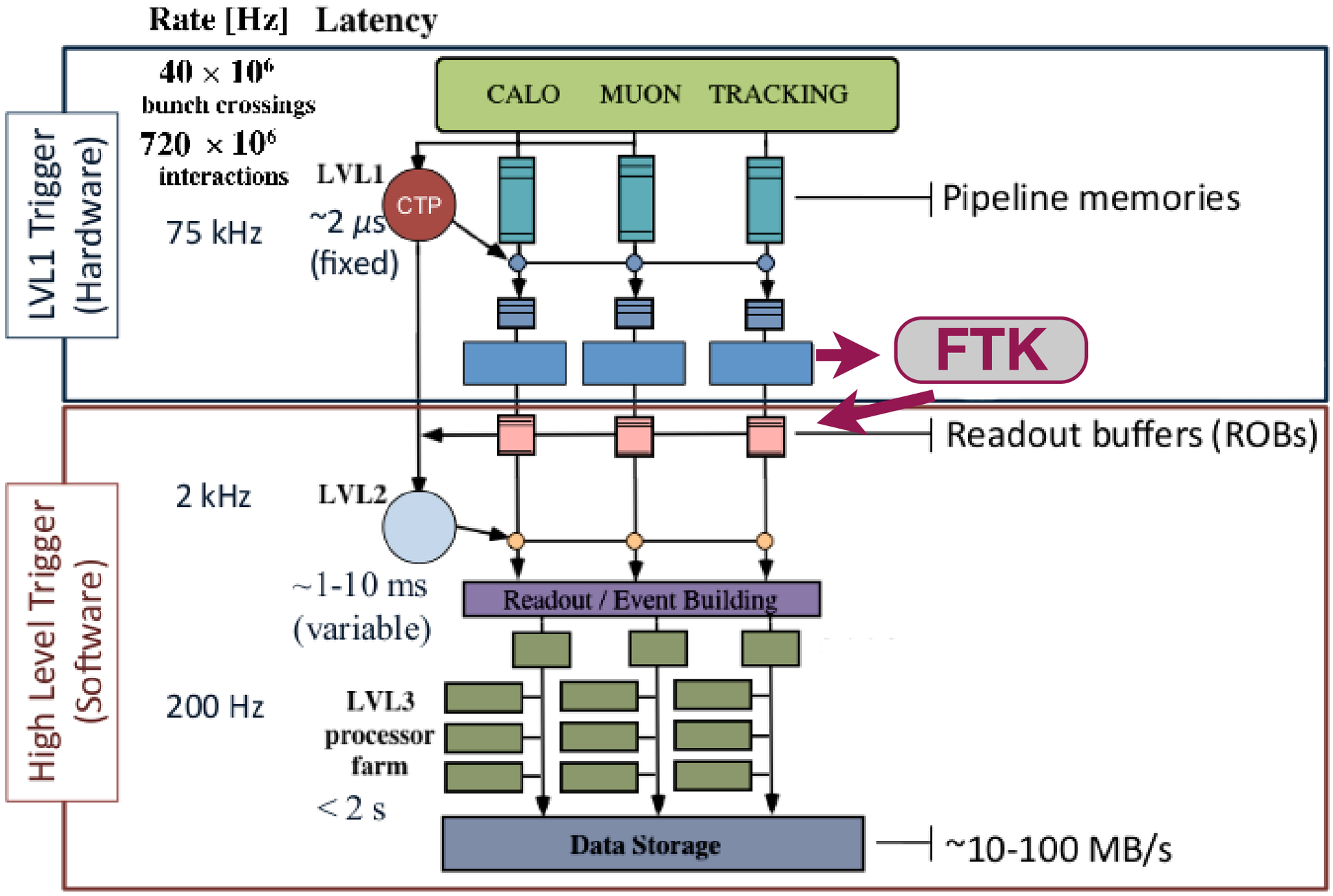


- Huge combinatorial problem, very non linear with number of interactions
  - Use algorithms in software run on CPUs: slow!
- FTK solves these problems with a hardware based approach

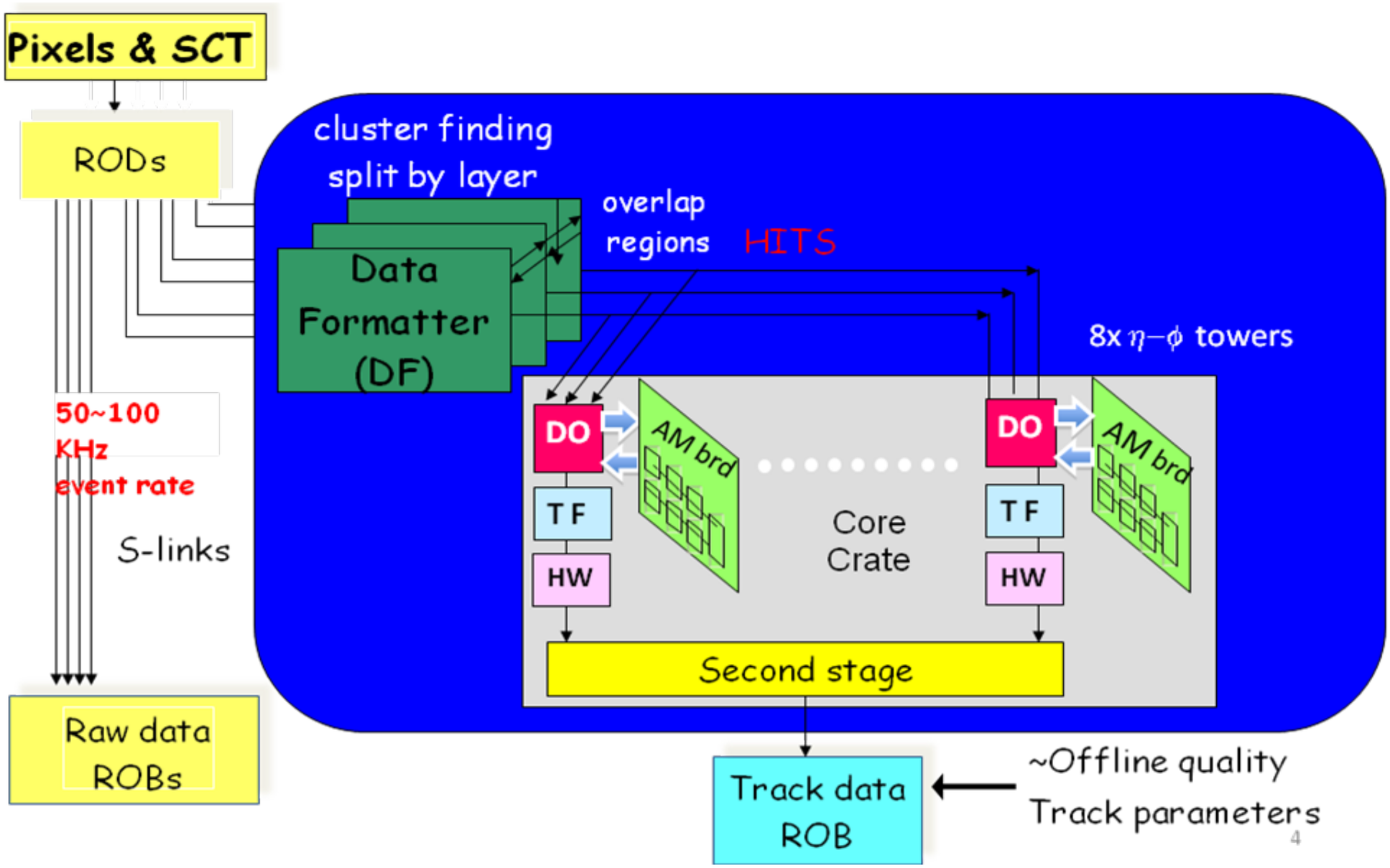
Conceptual Design

- Divide the detector η-ϕ towers: **Parallelize** the problem
- Convert clusters into coarse resolution hits: **Reduce** the data volume
- Compare hits to many pre-stored track patterns simultaneously: **Eliminate** costly loops
- Use a linearized fit for track candidates: **Simplify** algorithms
- All implemented in FPGAs or custom ASICs: **Hardware** solution

FTK in the ATLAS Trigger System



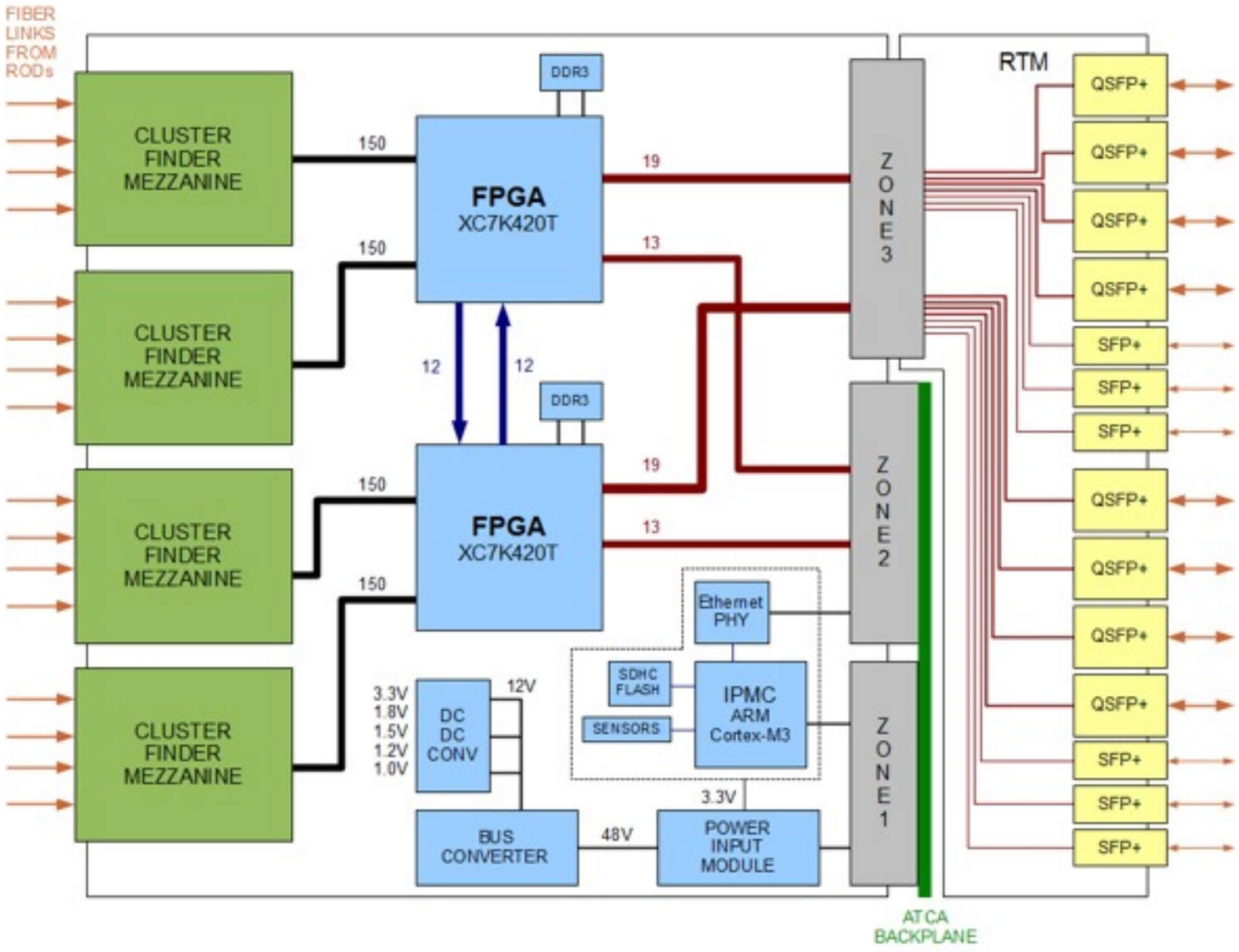
System Architecture



64 η-ϕ towers contained in 8 core crates

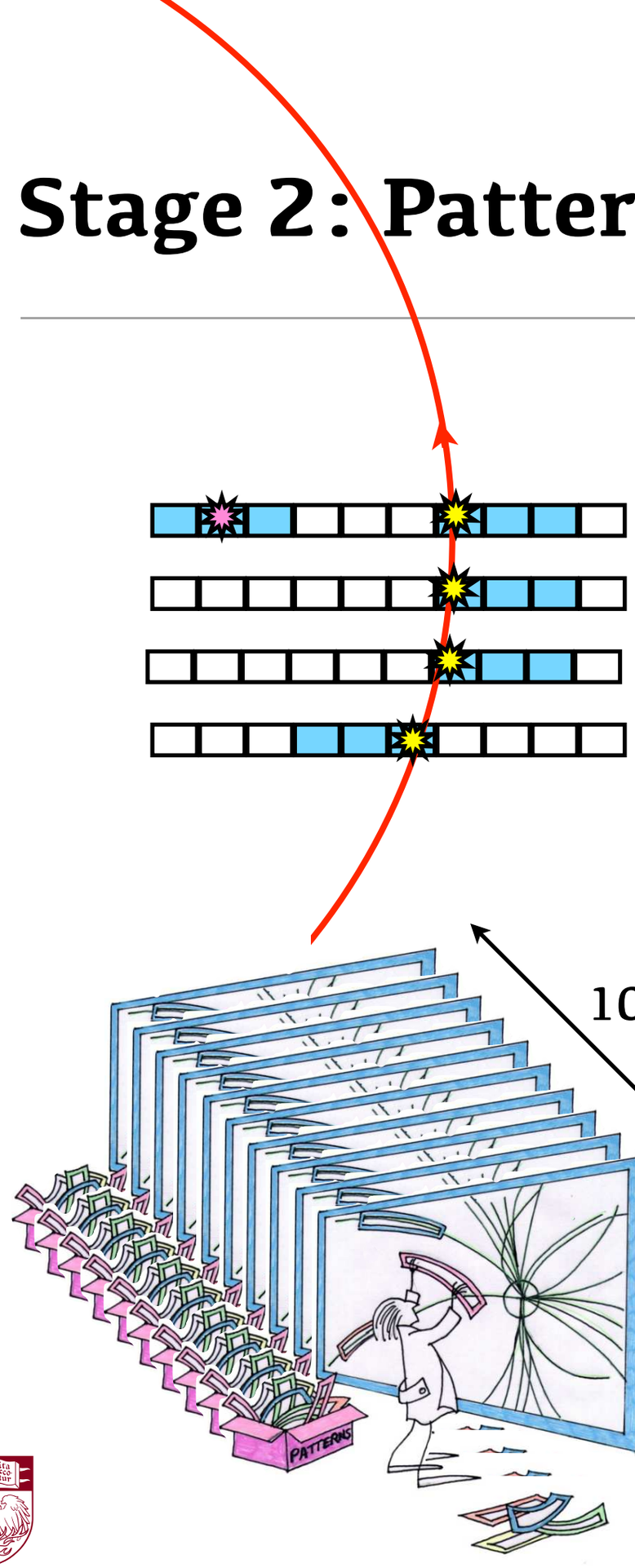
Stage 1: Data Formatting

- Receive data from silicon detectors
- Cluster pixel hits using sliding window algorithm in FPGA
- Route clusters to FTK processor units



- Implemented in ATCA crates with full mesh backplane
- 32 DF boards in X crates
- Each DF connects to 2 towers

Stage 2: Pattern Recognition



- Hits are ganged into Super Strips (SS)
  - Roughly 24x36 pixels/24strips per SS @ 46 int/x-ing
- **Custom associative memory chips** are used to compare hits to $O(10^9)$ patterns **simultaneously**
  - Pattern matching finished as soon as all hits are read
- Matched patterns (Roads) are then fit to reject bad roads
  - Most matches are fake, need fits to reduce bad rate

Content Addressable Memory

- Associative memory chips based on CAMs
- Data comes in, address comes out
- No memory of previous matches

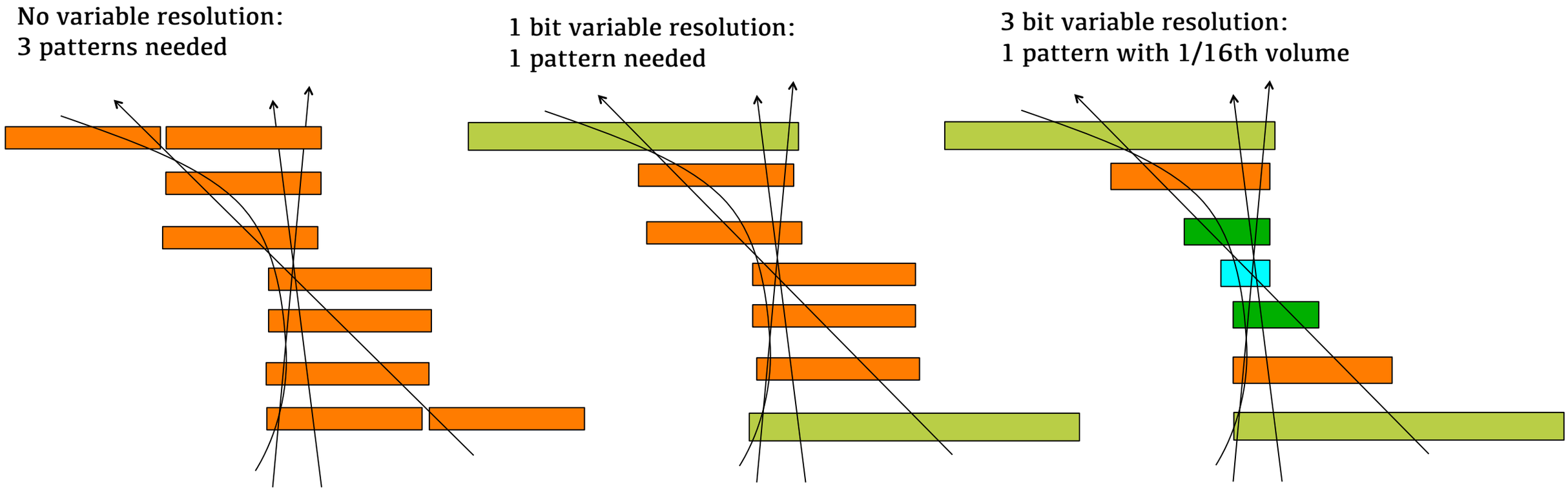
Pattern Recognition Associative Memory

- Allows hits arriving at different times (but same event) to be compared!

animation by Fermilab engineer Jim Hoff

Refinements

- Majority Logic: Only require N out of M layers have a match
  - Gains efficiency
- Variable Resolution Patterns (Don't Care Bits)
  - Reduces the number of patterns and fake matches



- Number of don't care bits set on a layer by layer, pattern by pattern basis

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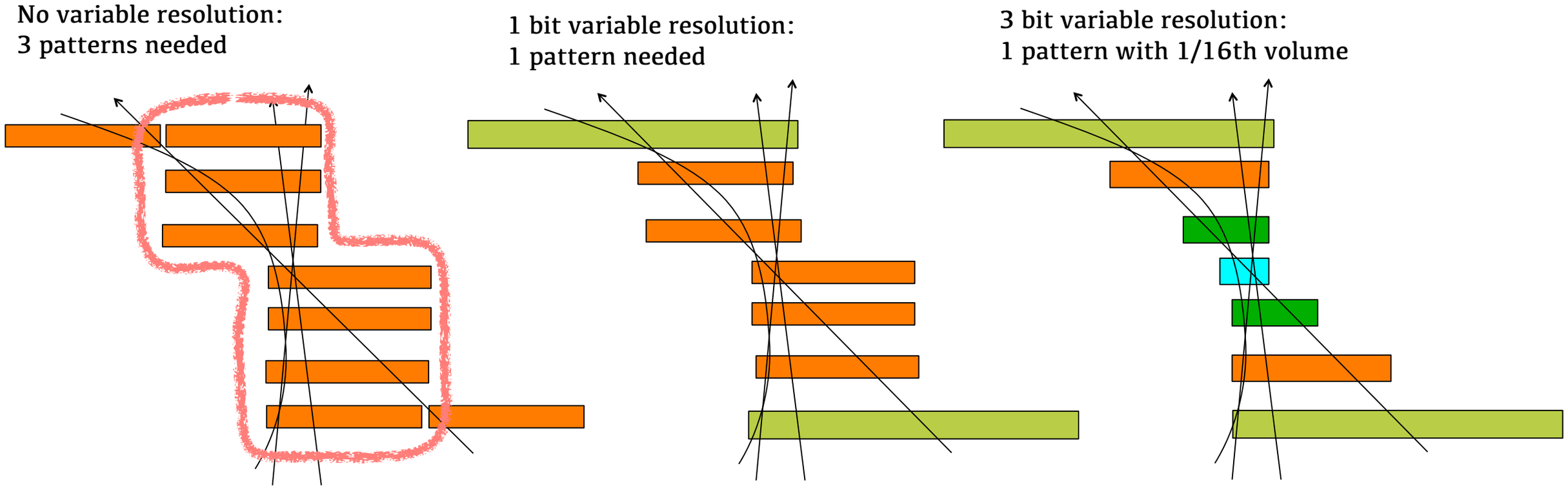

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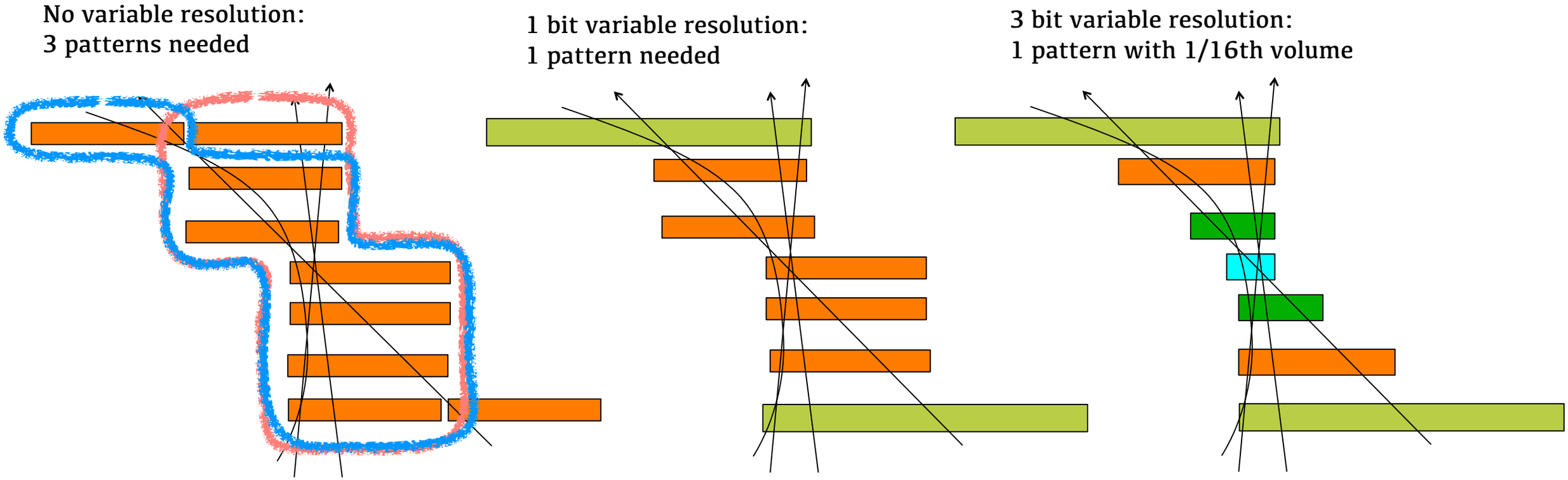

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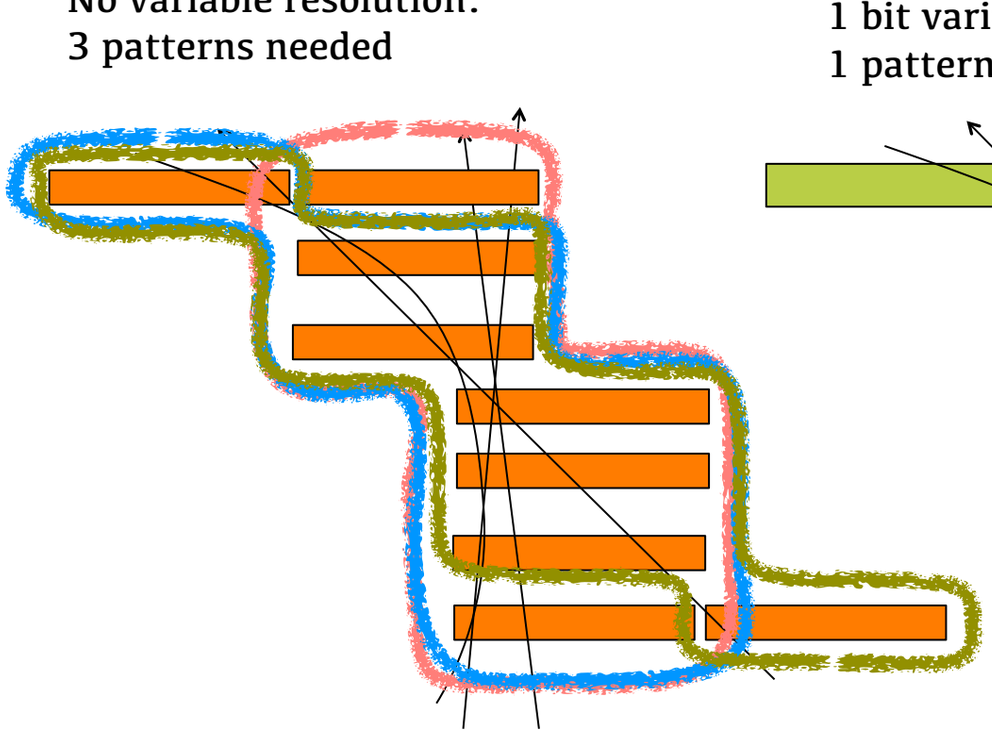
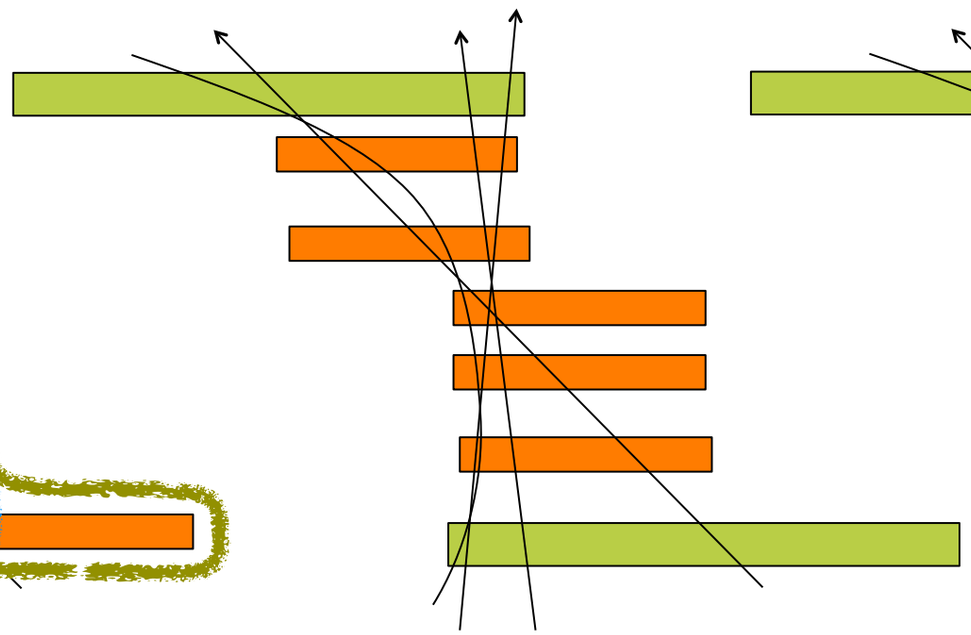
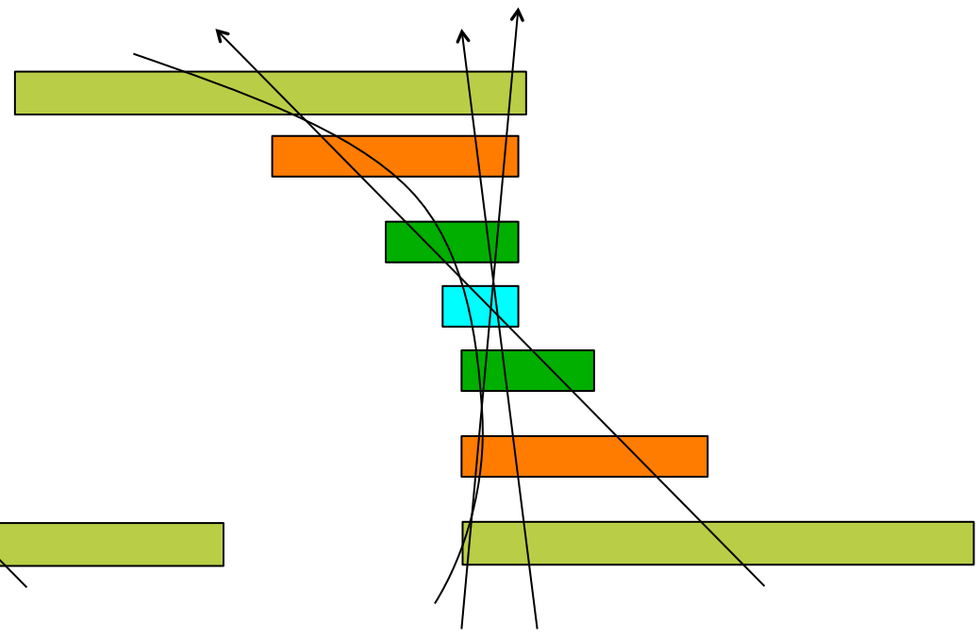
No variable resolution:
3 patterns needed



1 bit variable resolution:
1 pattern needed

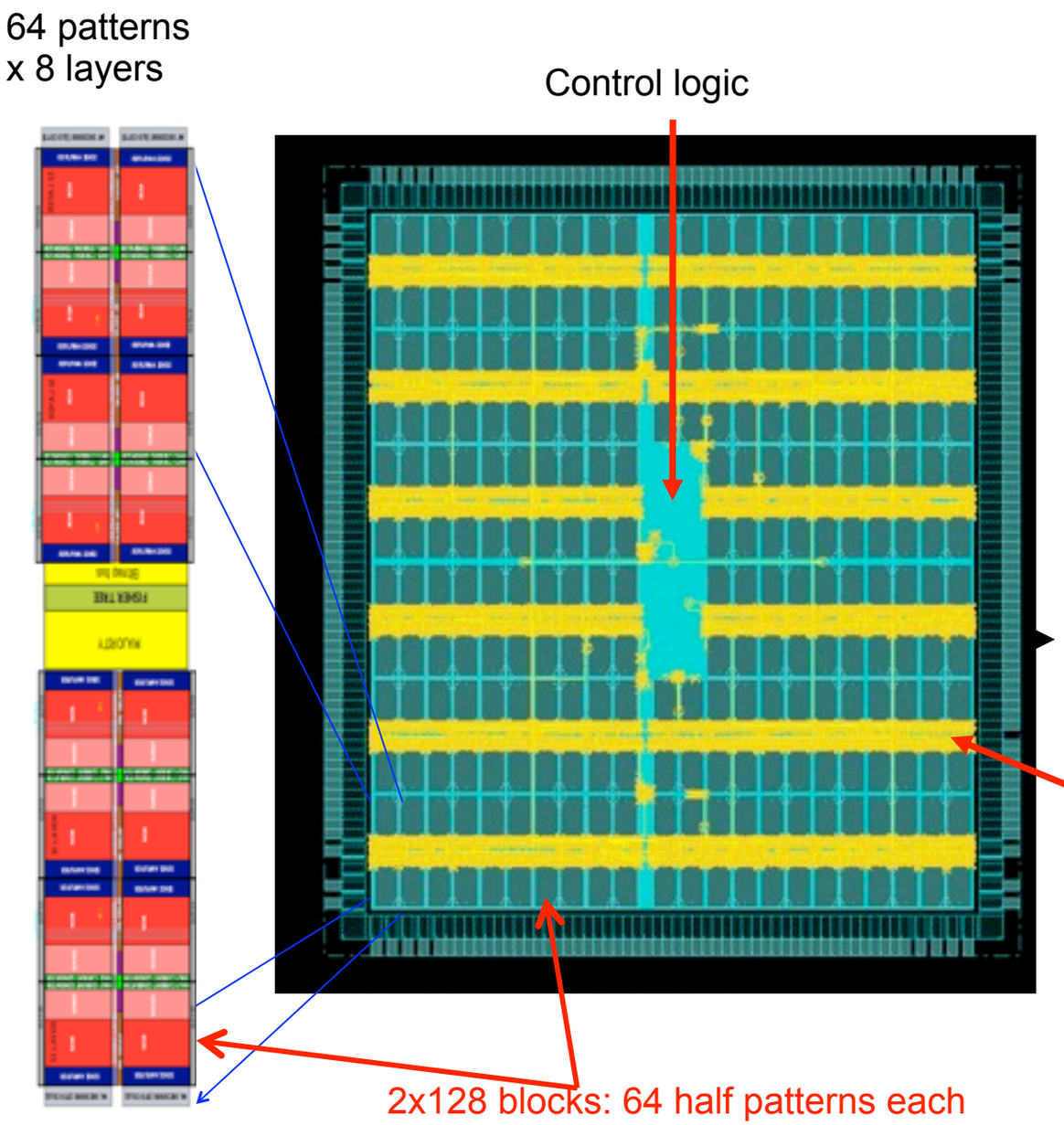


3 bit variable resolution:
1 pattern with 1/16th volume



- Number of don't care bits set on a layer by layer, pattern by pattern basis

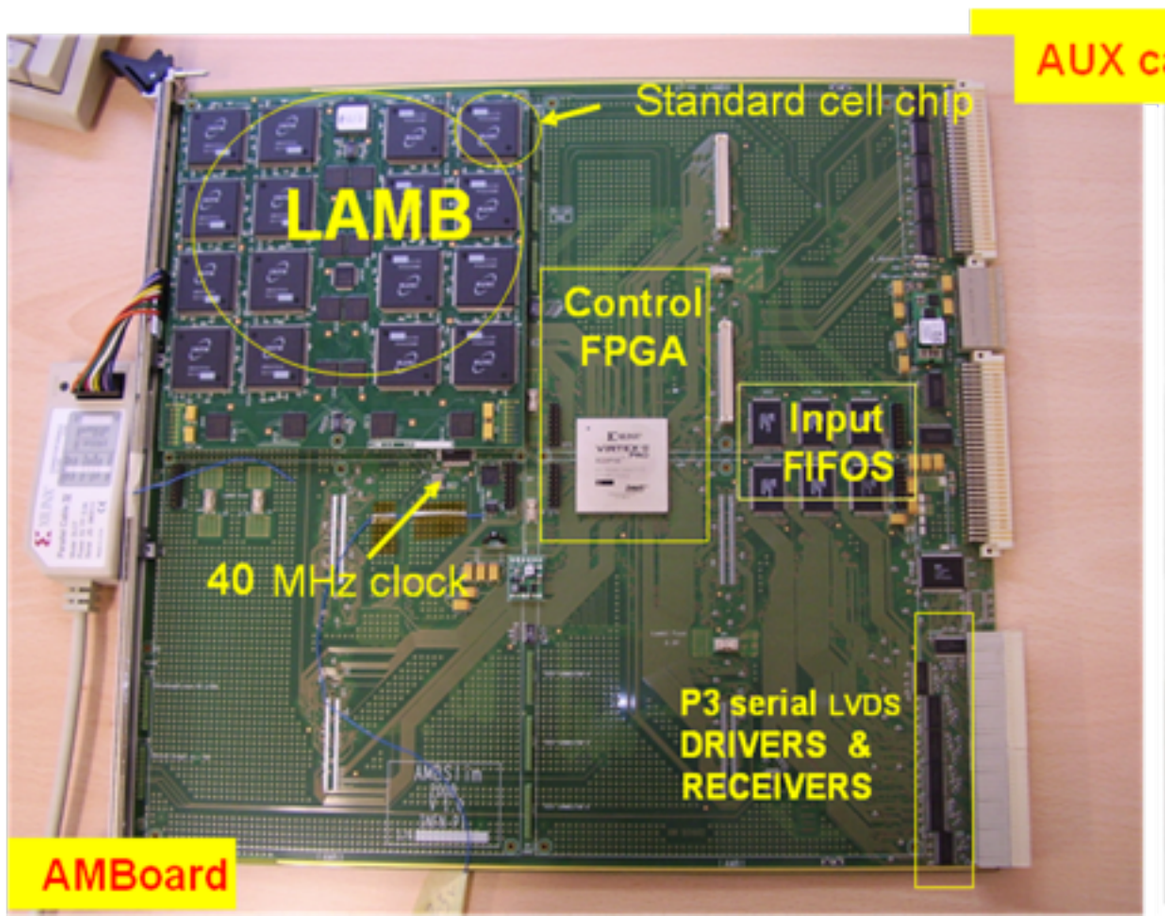
AMChip04

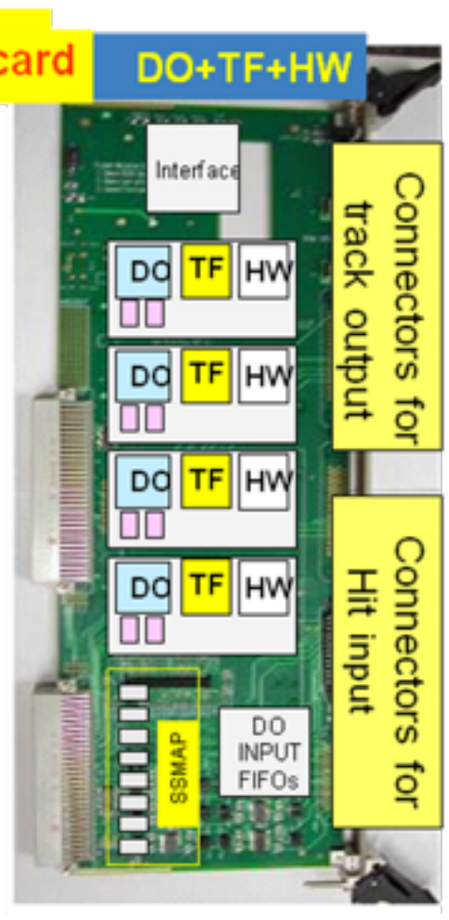


- AMChip04: 64 nm fully custom associative memory chips with up to 80k patterns
  - 8 Layer (Pix + 4 axial SCT + 1 stereo SCT)
  - 3-6 bits for variable resolution patterns
  - Low power design: ~2W/chip, a factor 30-50 reduction in power/pattern/MHz over predecessor SVT chip

AM Board

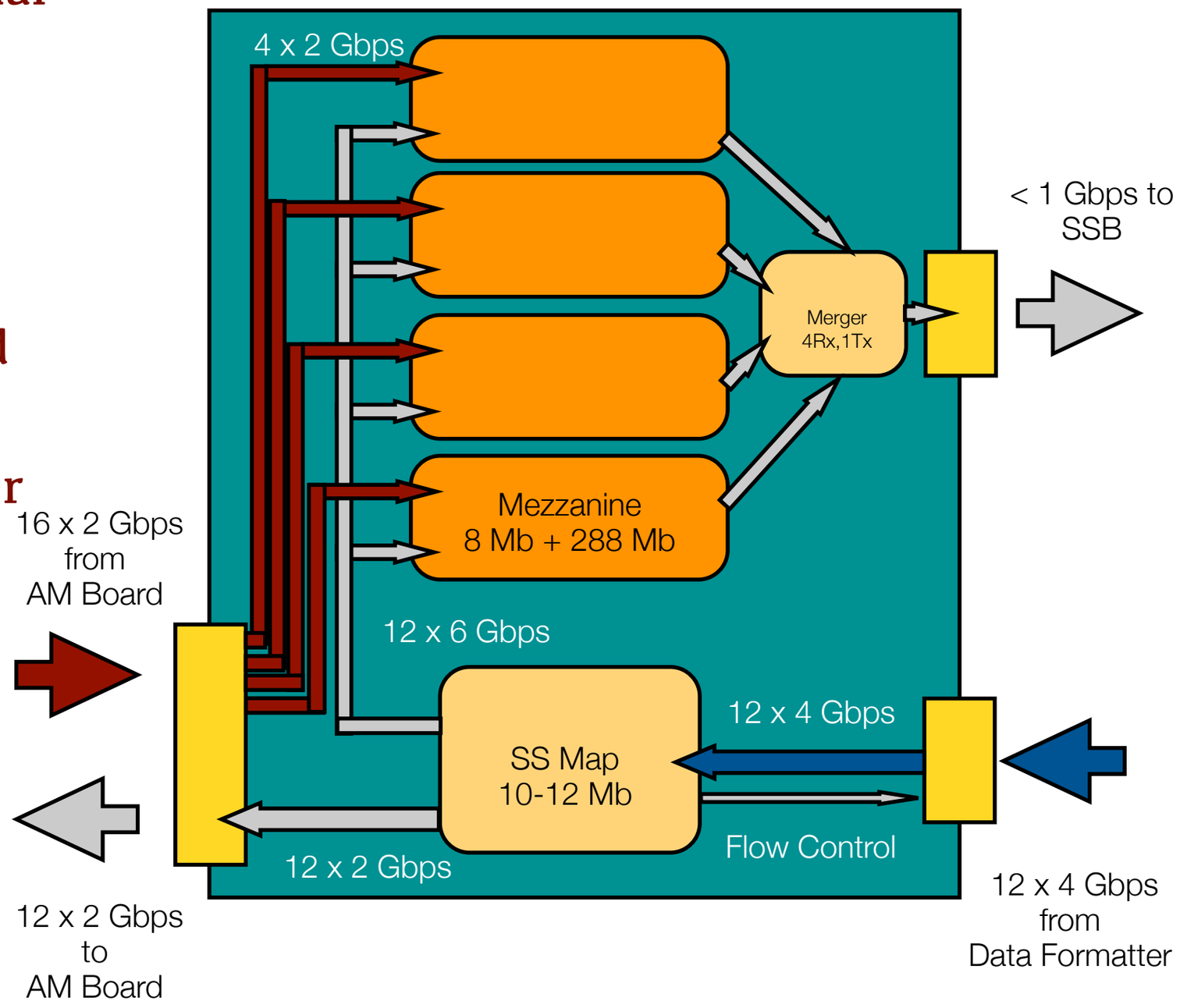
- AM Chips mounted on 4 large mezzanines
  - 128 Chips total
- 2 boards per tower, 16 per core crate
  - Each weighs 2 kg!
- Data send from Auxiliary card to motherboard over P3 connectors





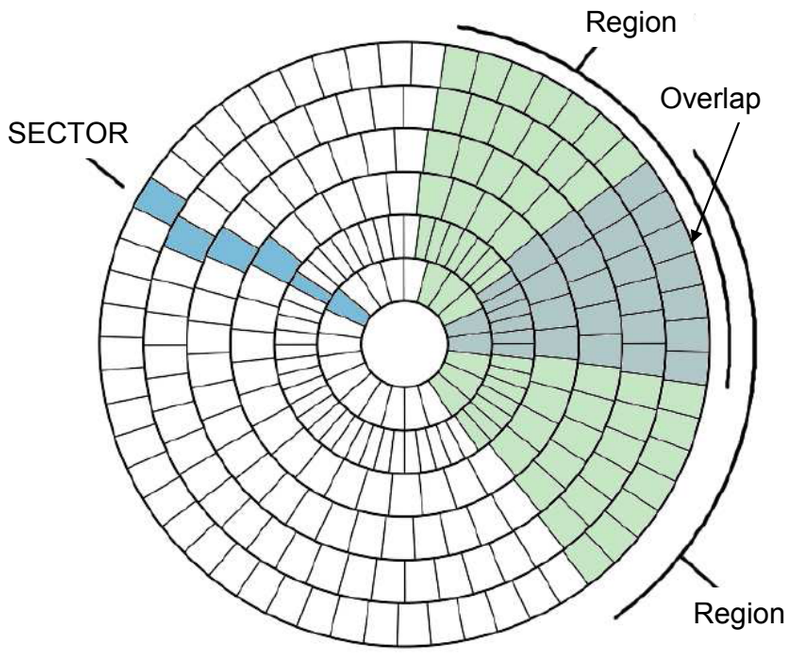
The AUX Card

- The AM Board has multifunctional Auxiliary Card
- Converts clusters to SS
- Receives matched road IDs and fetches full resolution hits
- Performs 8 layer fit to reject bad roads
- Sends roads to board for 11 layer fit



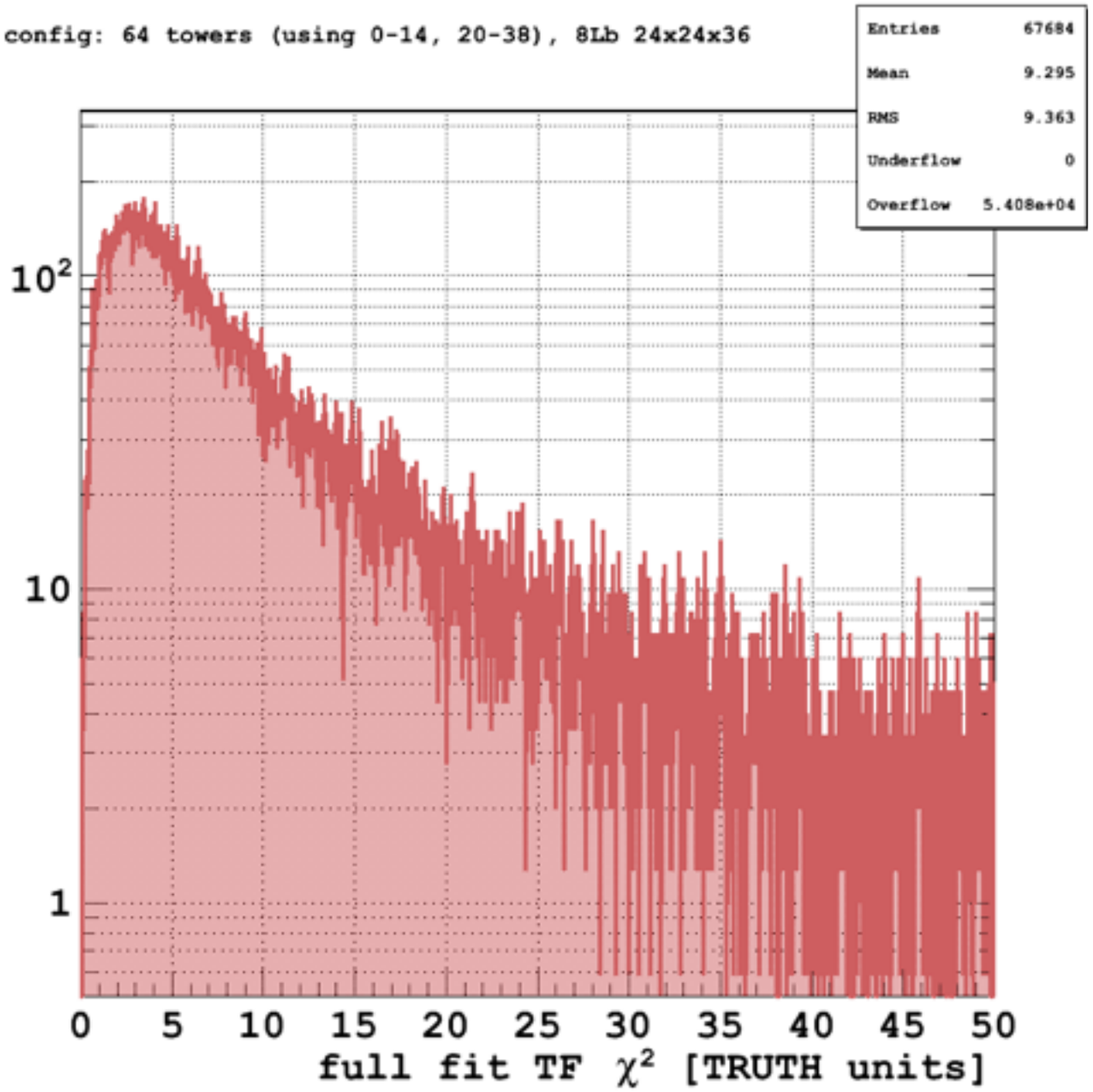
Linearized Track Fitting

- Fit constants predetermined and defined by sector
- FPGAs multiply and add coordinates by constants to get χ^2
- If a layer is missing, missing hit position is guessed so χ^2 can be calculated
- Keep roads with at least 1 good track
- Fit 1 track / ns!

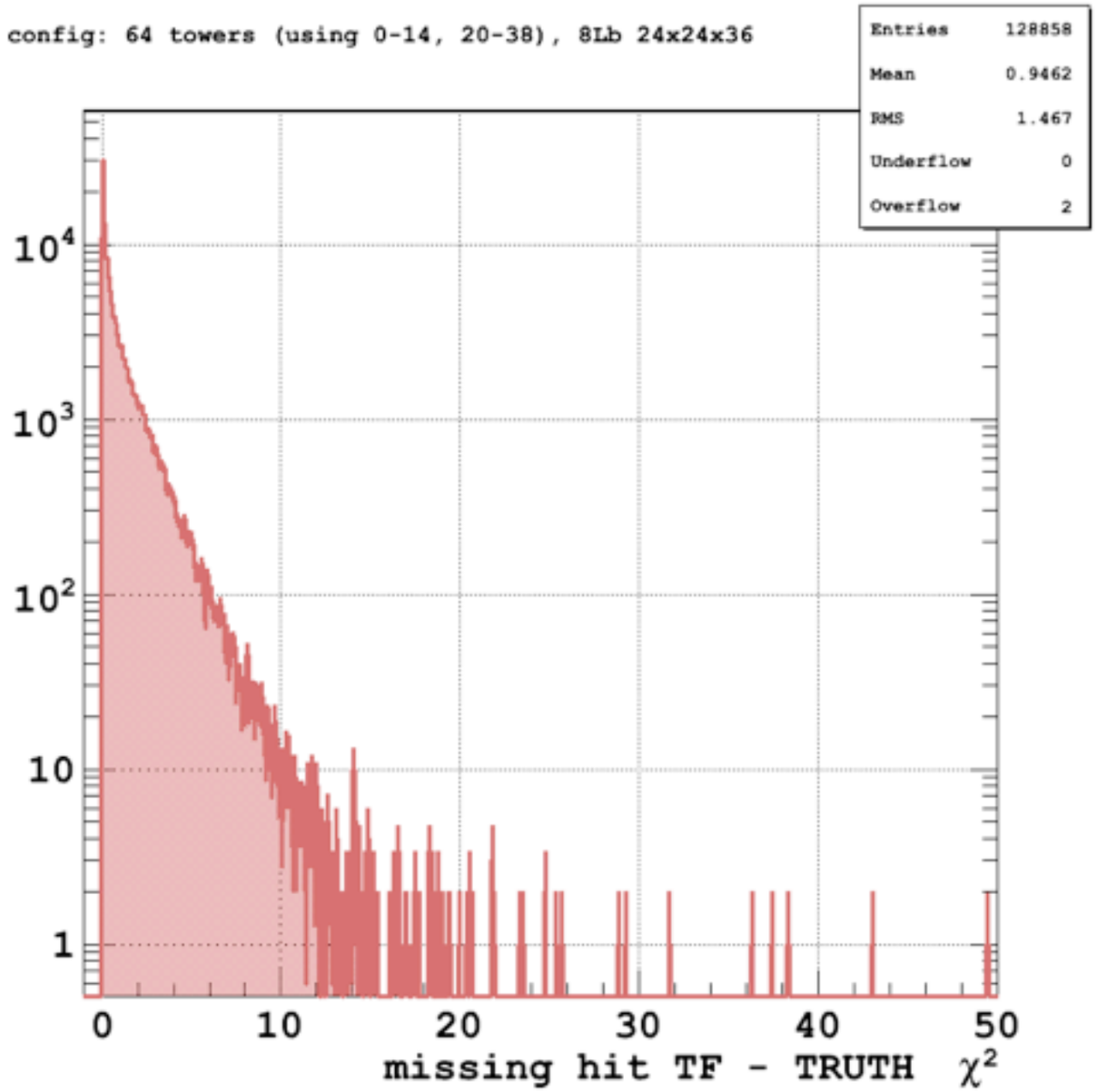


$$\chi_i = \sum_{j=1}^{N_c} S_{ij} x_j + h_i; i = 1, \ldots, N_\chi$$

Fitter performance



χ^2 for single muons

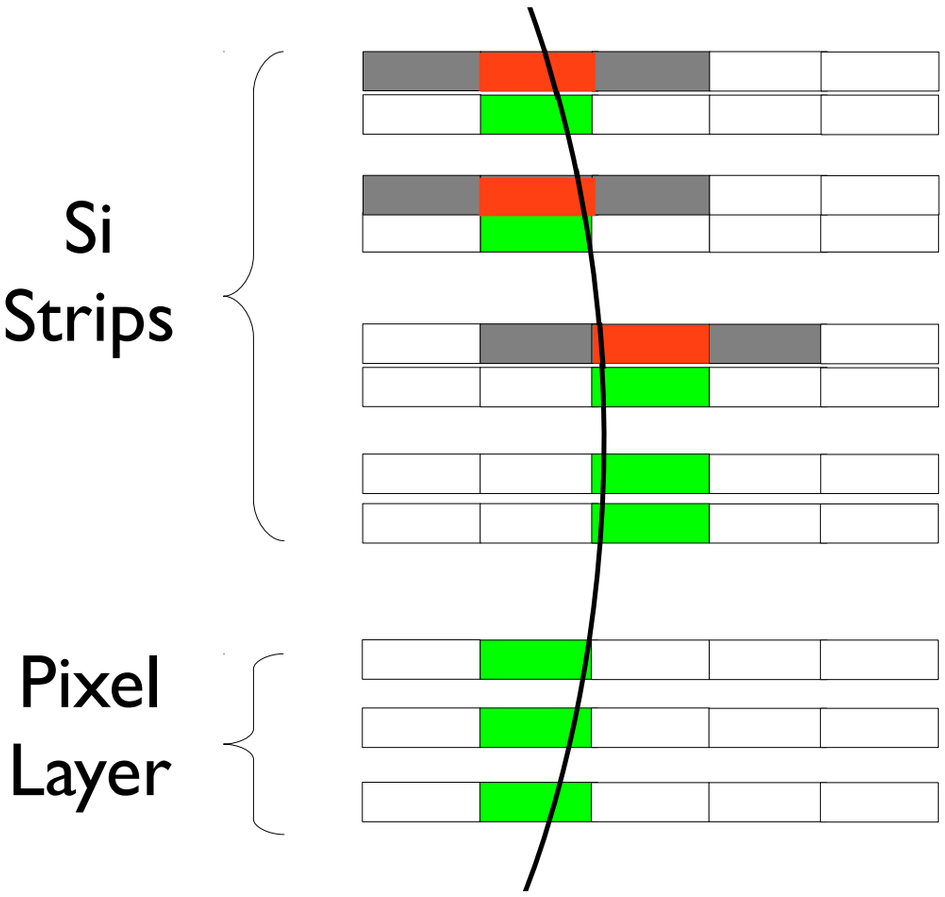


$\Delta\chi^2$ for single muons when missing hit is guessed

Stage 3: 11-layer Track Fitting

- Use constants precomputed from linearized constraintsto guess hit coordinates

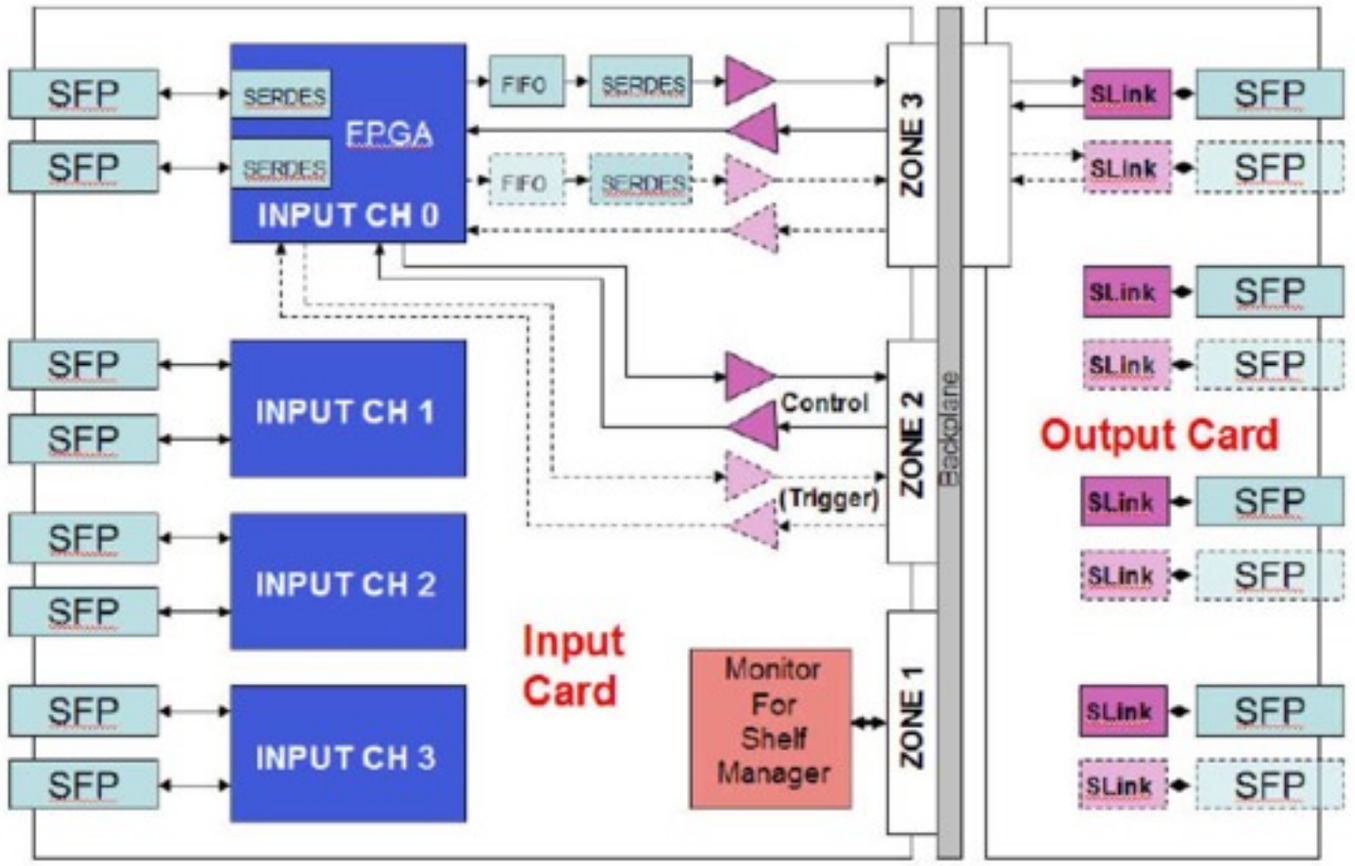
$$x'_i = \sum_{j=1}^{11} H_{ij} x_j + g_i; i = 1, \ldots, N_\chi$$



- Find matching SS
- Refit with good hits to find best χ^2
- Good tracks, with parameters, hits and errors are sent to final crate for formatting for L2

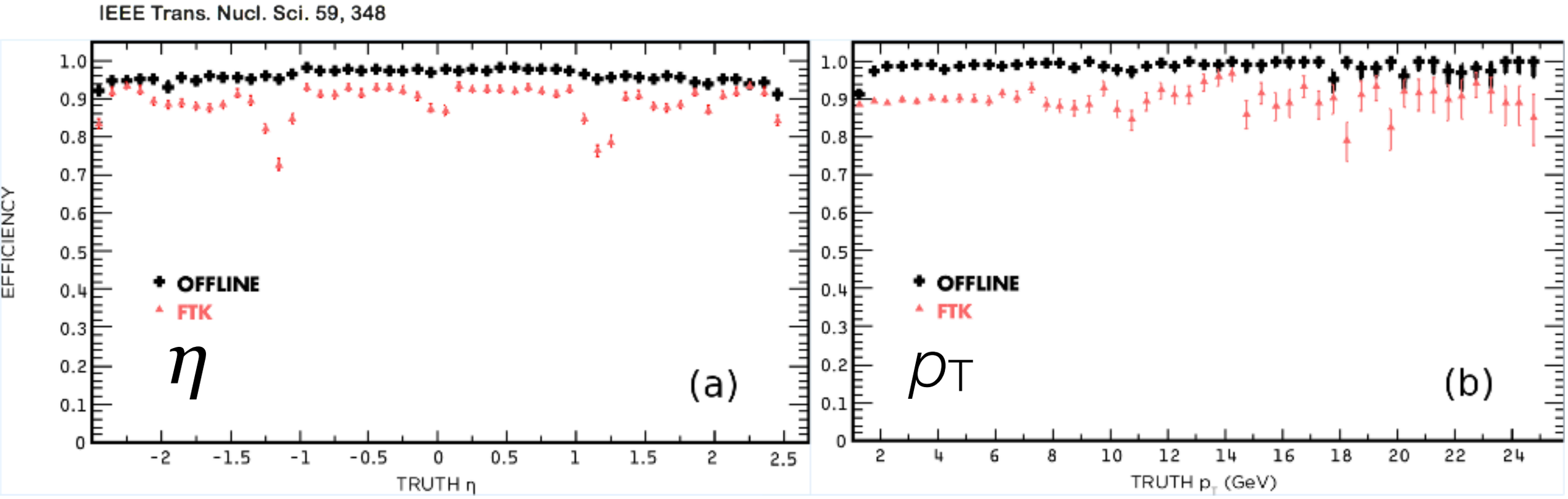
FTK to Level 2

- FTK to Level 2 Interface Crate connects FTK to HLT
  - Formats data for HLT
  - Also does monitoring and control
- Uses dual-star ATCA crate
  - Will allow for local trigger processing (primary vertex finding, beamspot, MET, etc.) in the future



Performance: Efficiencies

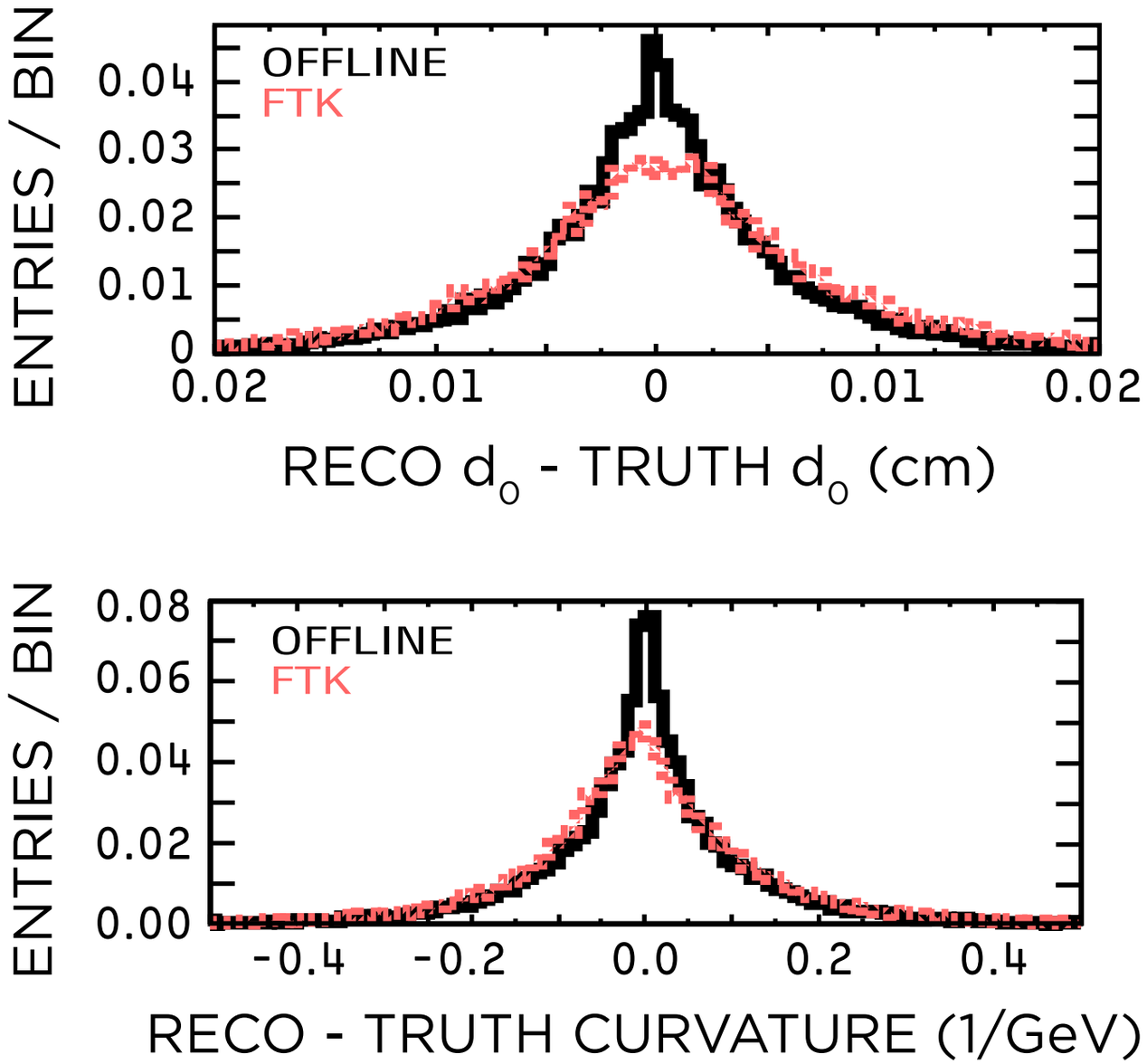
- FTK has a detailed simulation of system logic for design and performance studies



Tracking Efficiency for Single muons

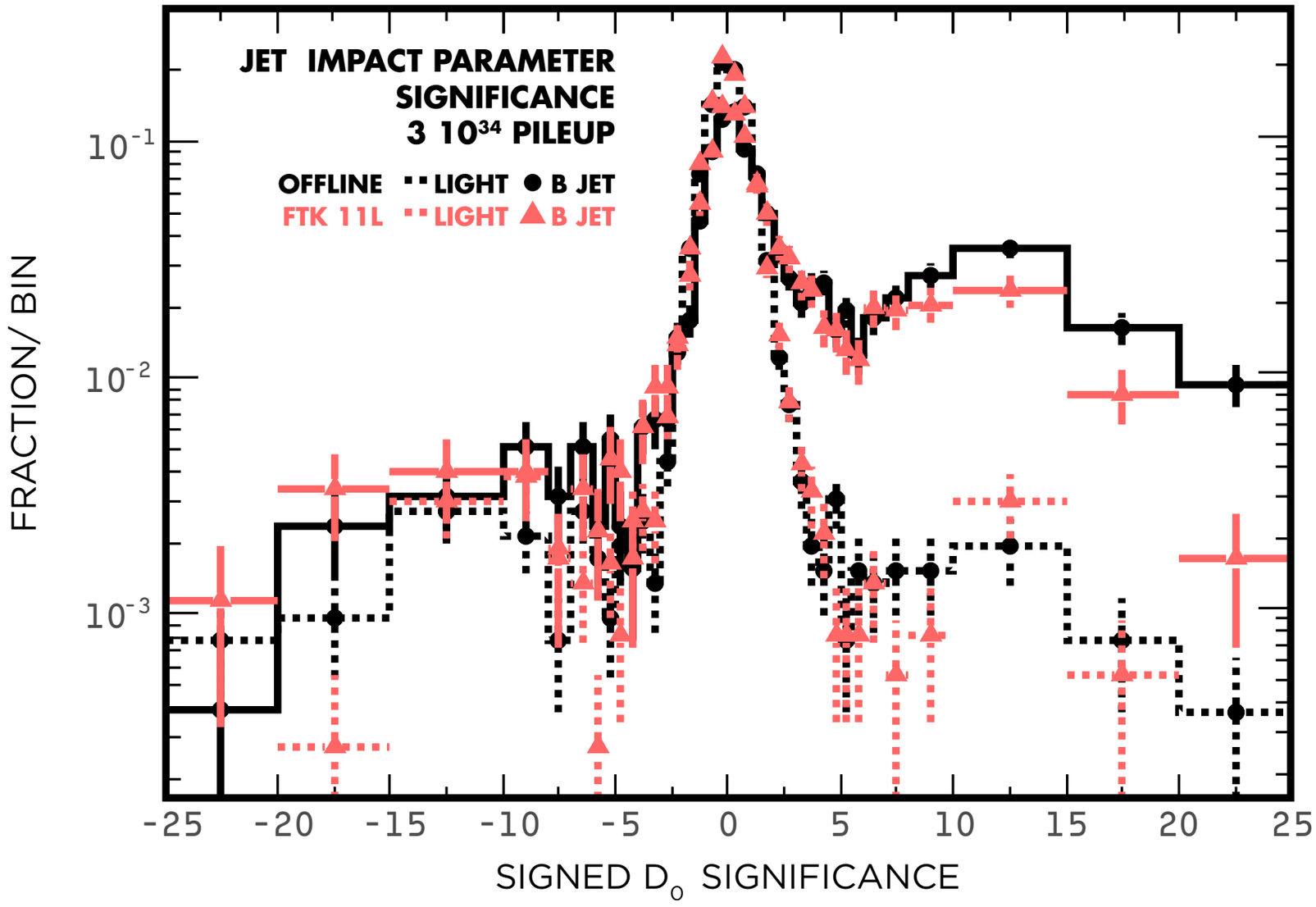
Performance: Resolutions

- 11-layer linearized fit gives similar resolution to offline software

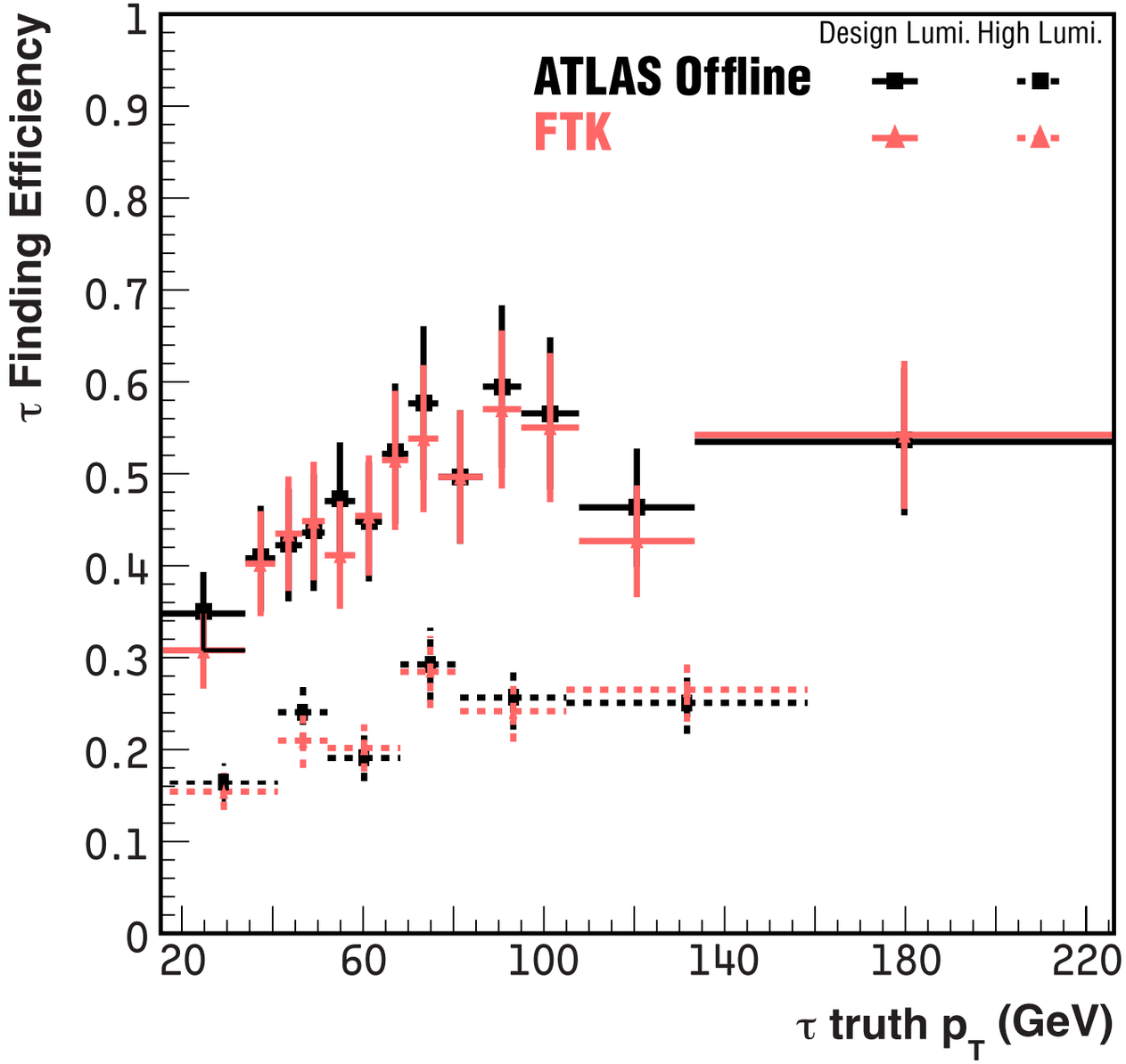


Performance: Secondary Vertex Tagging

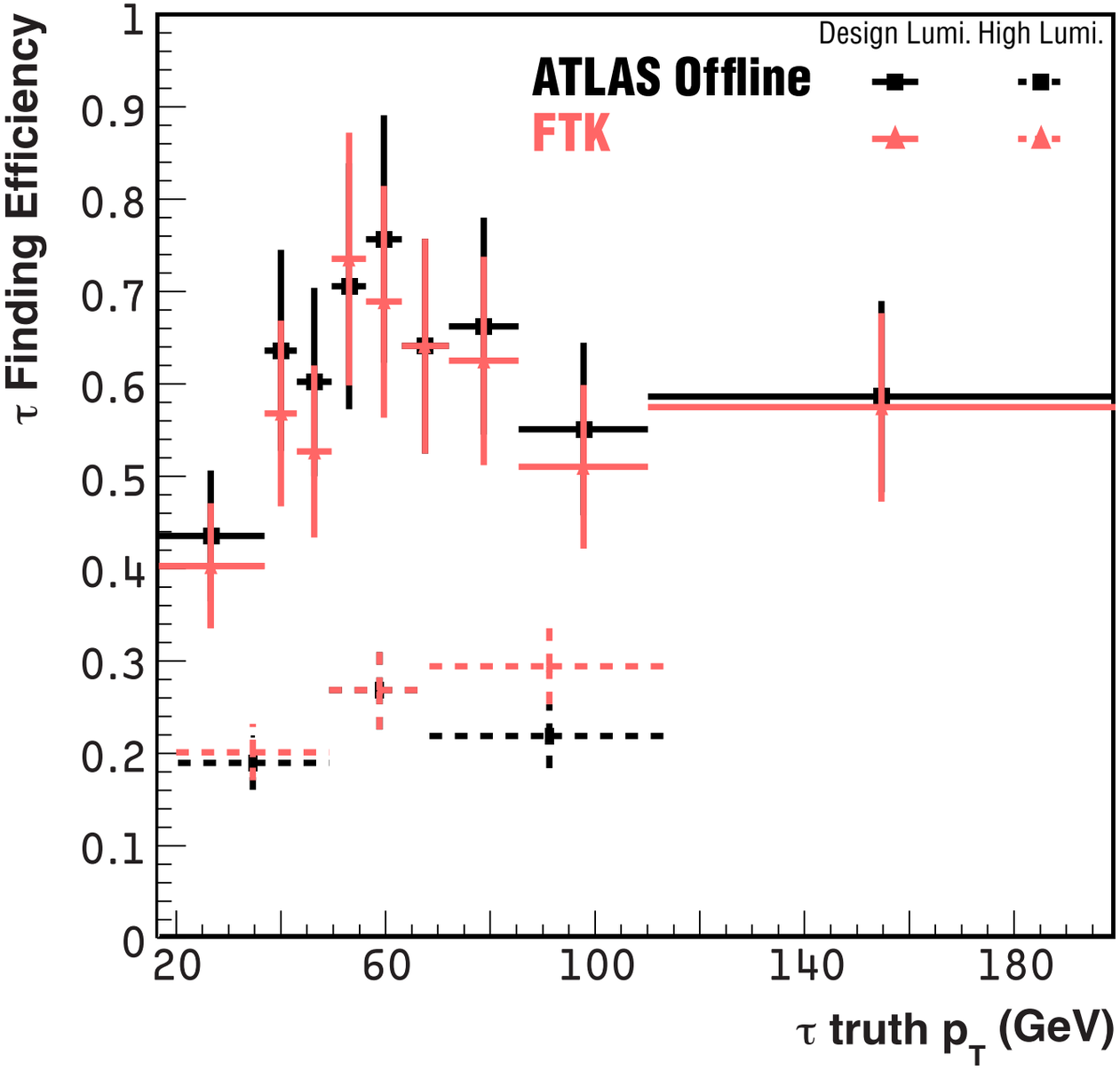
- Signed impact parameter significance has good light quark rejection



Performance: Taus

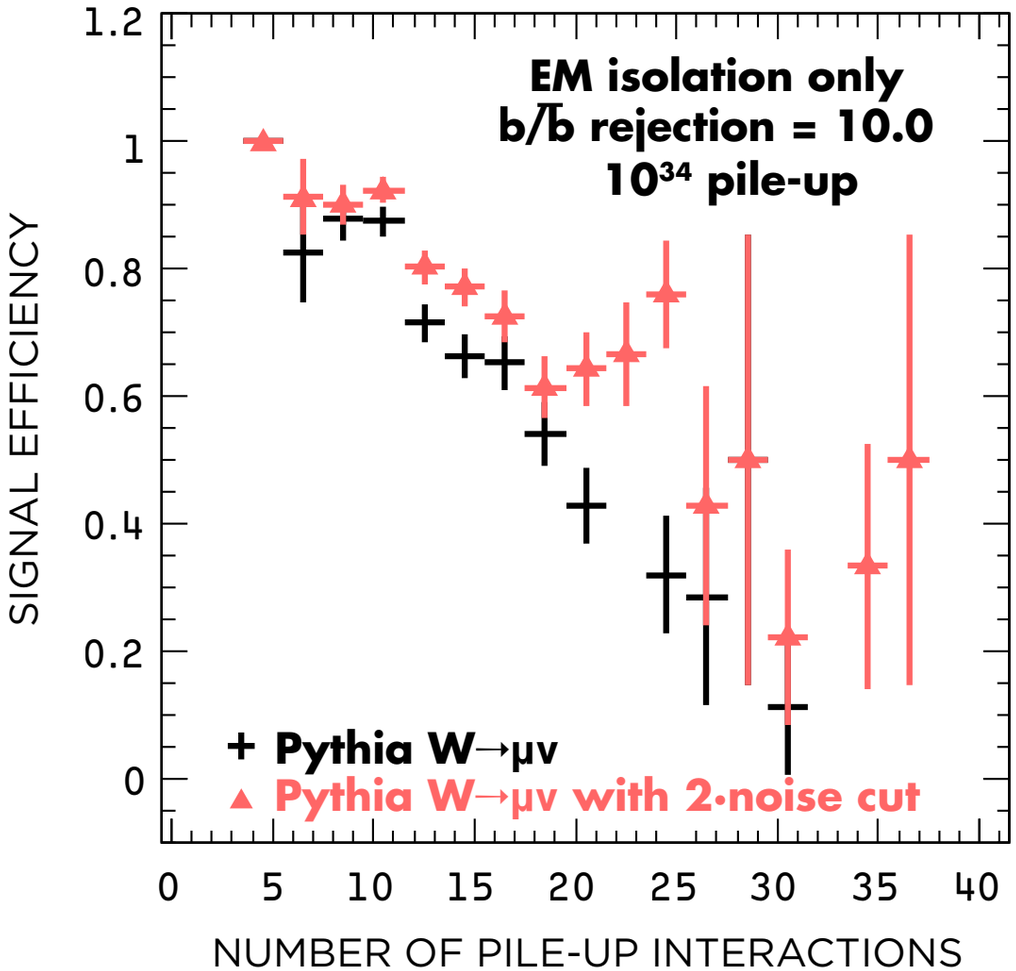


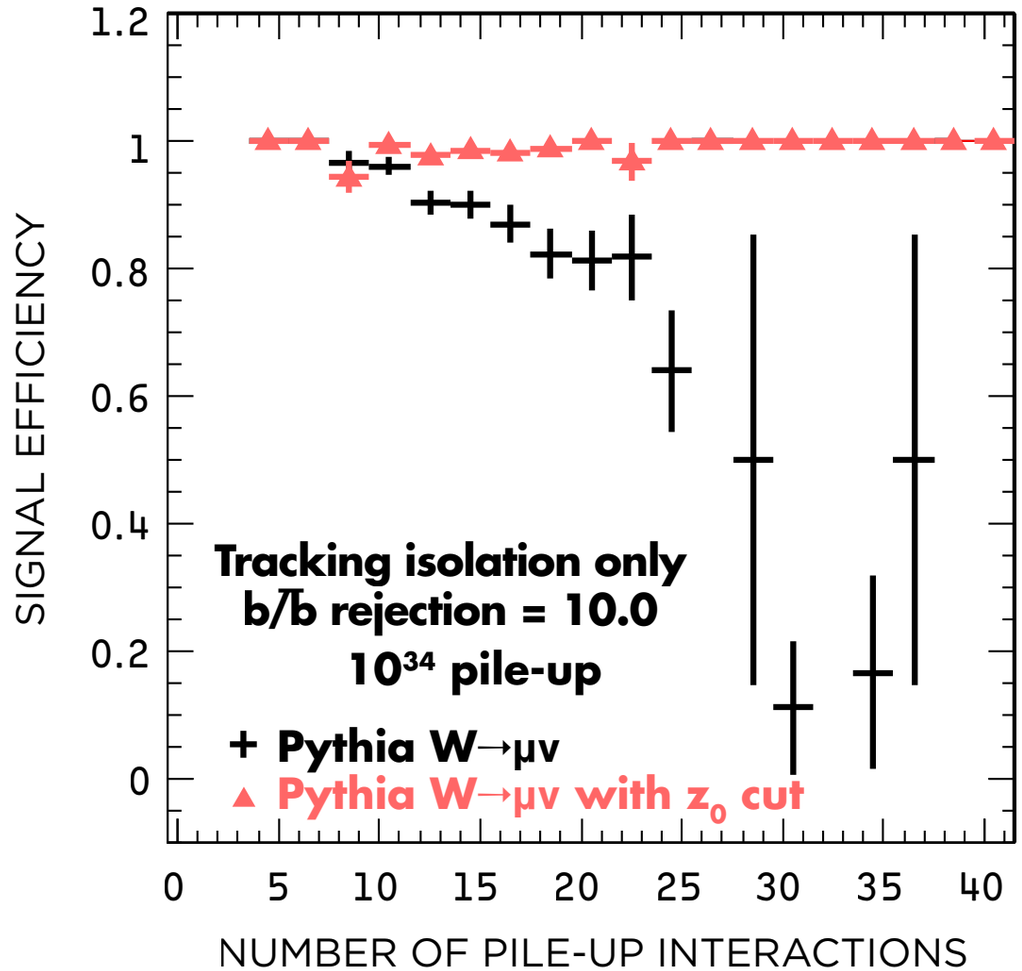
1-prong



3-prong

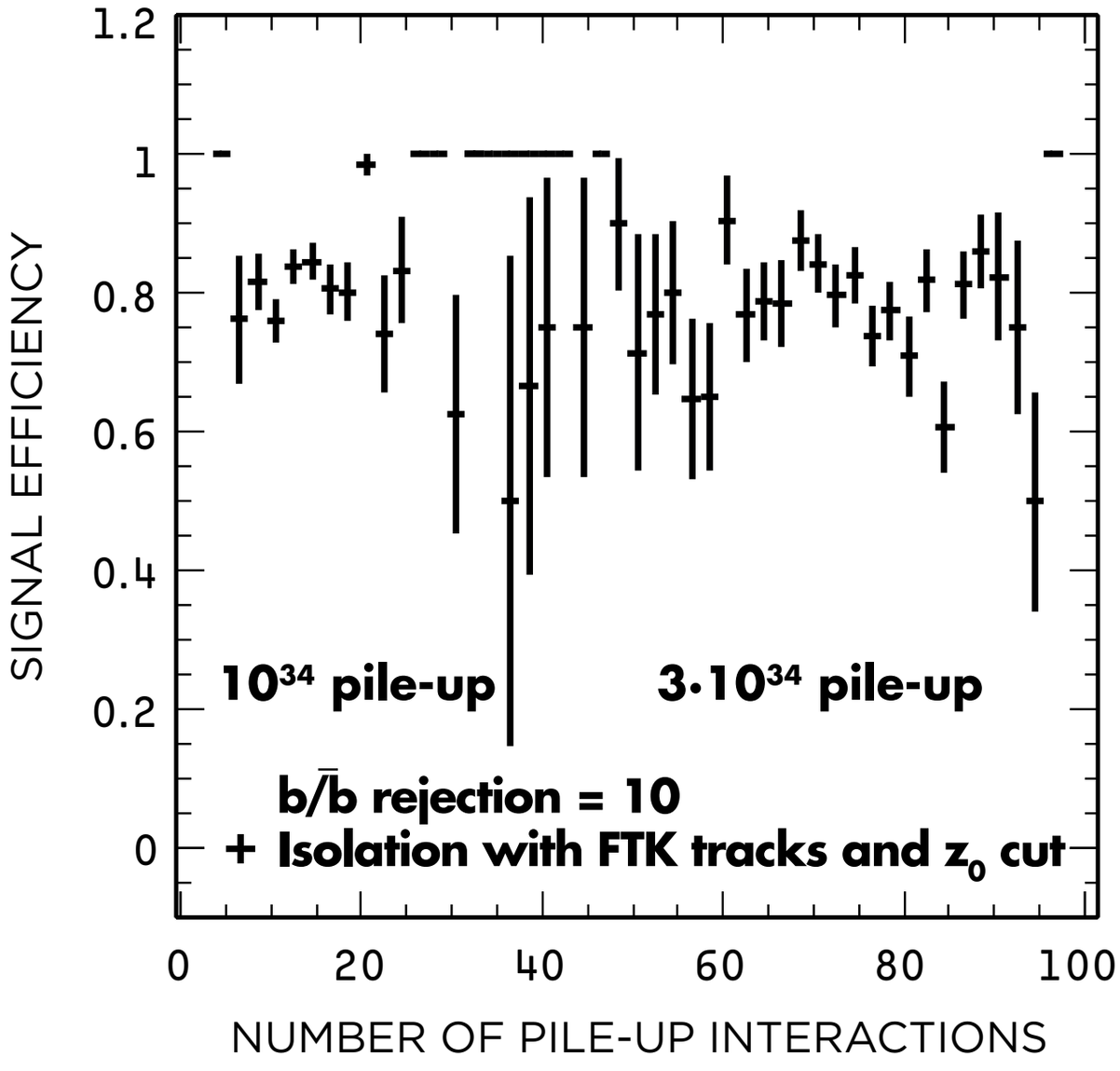
Performance: Isolation





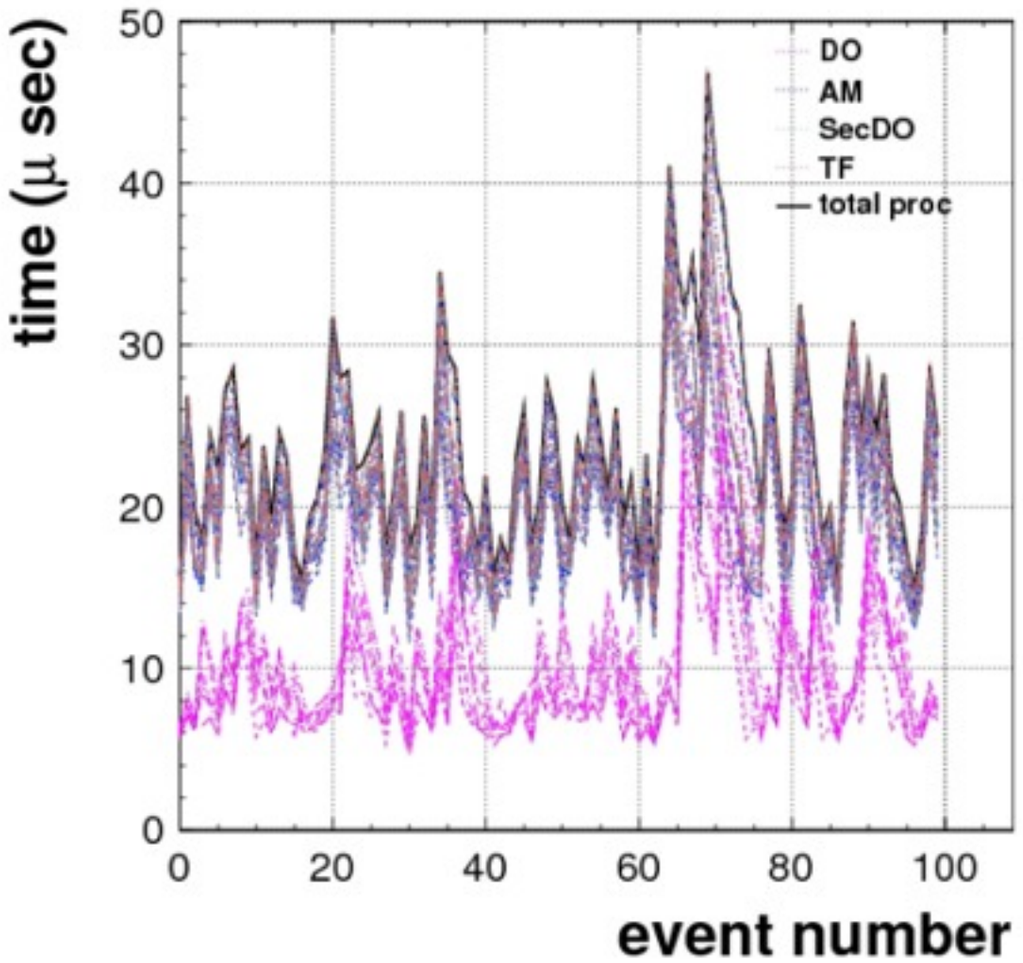
Performance: Isolation Trigger

- Efficiency for W➔μ ν with isolated muon trigger

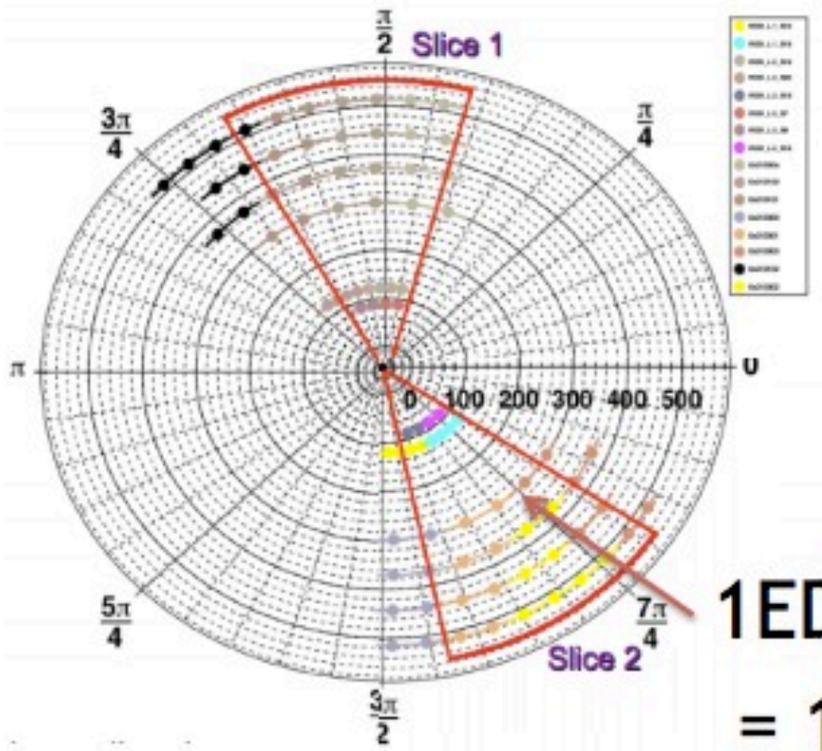


FTK Timing

- At $3x10^{34}$ average processing time for full detector is 25μs
- L2 ROI processing is O(10ms)
- Majority of time spent in AM, DO
  - Dominated by transfer of SS/hits
- Based on timing simulation with estimates on how long each board processes a word



Phase 0: Vertical Slice Test



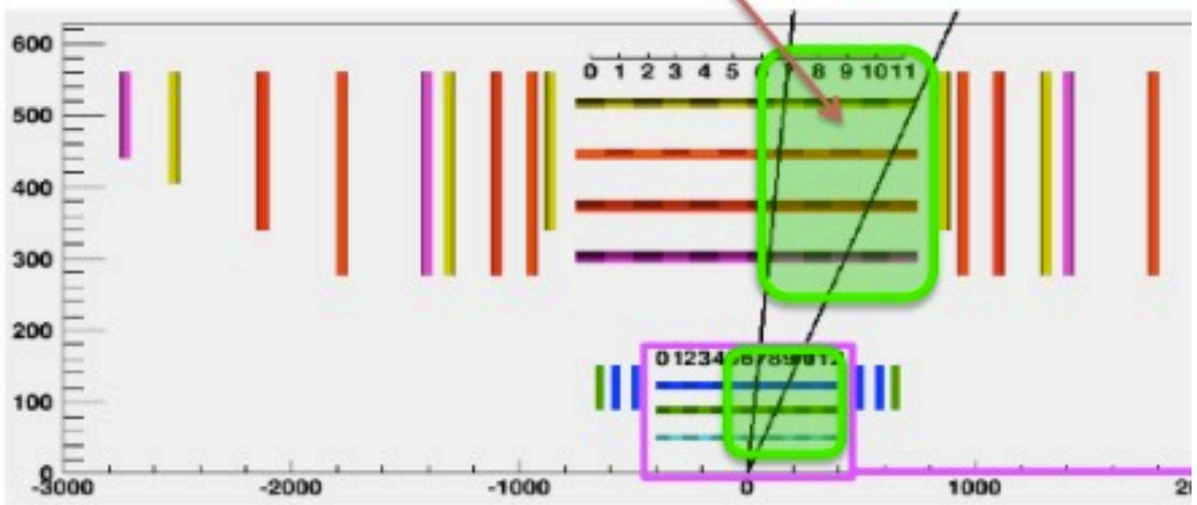
4 pix (L1, L2) + 4 SCT

RODs per tower ($0.3<\eta<1.15$)

Total 16 ROLs for 2 towers

1EDRO+1AMB

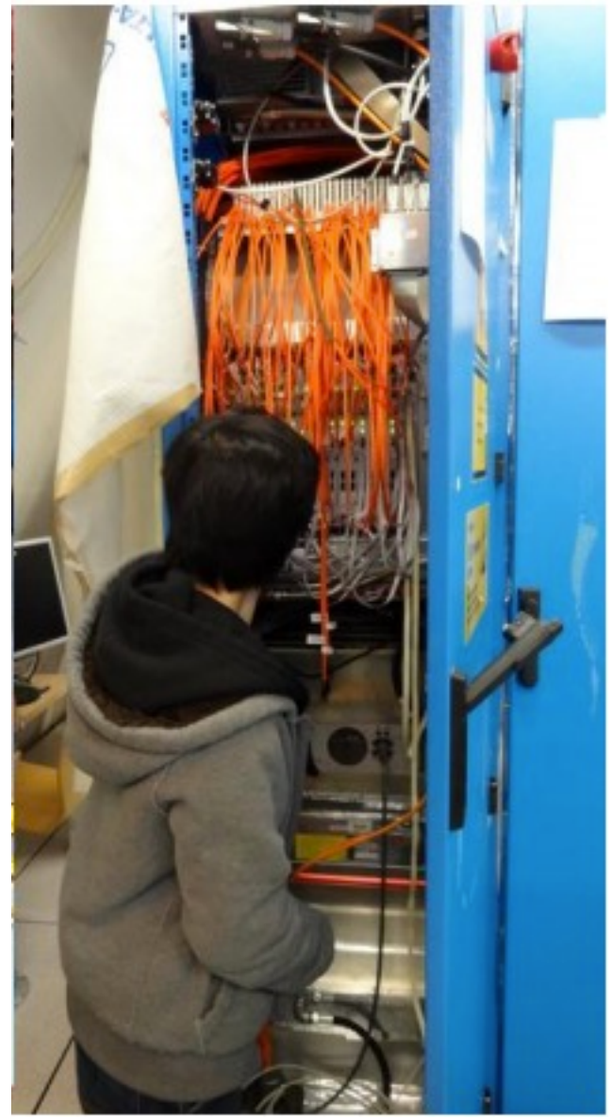
= 1 tower

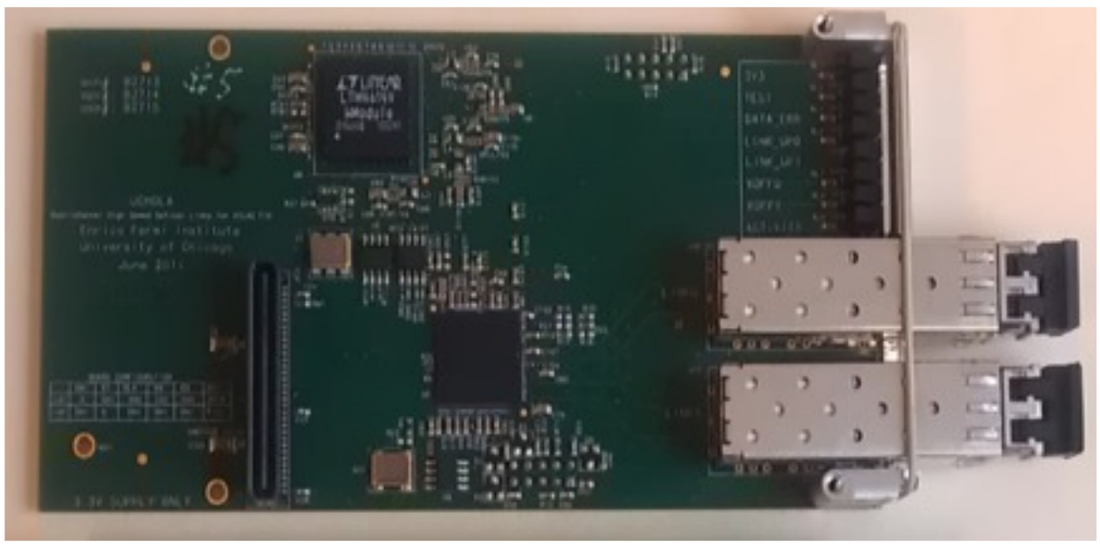


15-05-2012

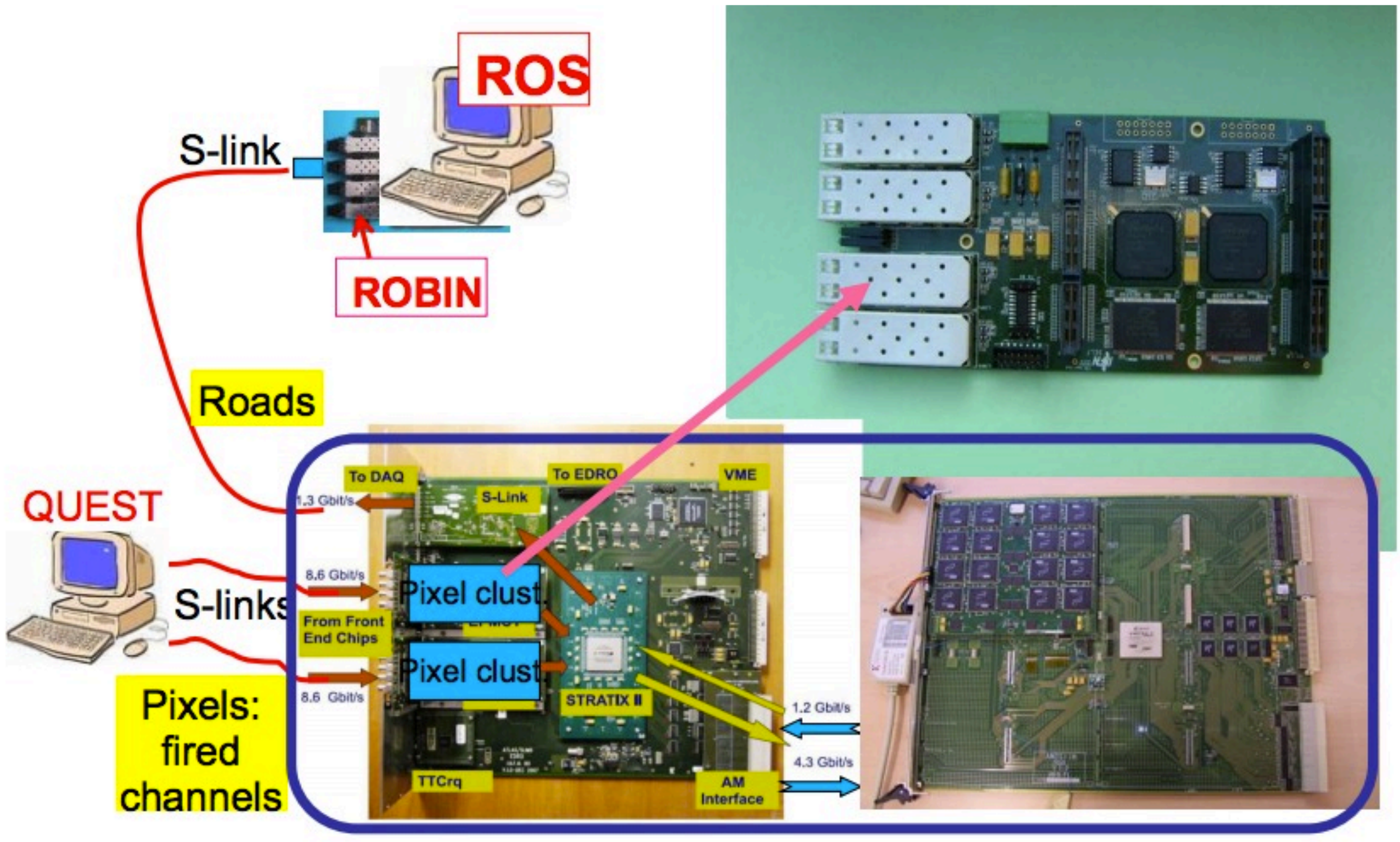
Dual-Output HOLAs

- One part of the Vertical Slice is installed at P1 this January: Dual output HOLAs
- Replaces HOLAs for RODs in the vertical slice with ones that have two outputs:
  - ROS : standard behavior
  - FTK : Can exert flow control when FTK is enabled
- Produced and Tested at Chicago in Nov/December, 32 installed and tested at P1 since January
  - Only 2/270 failed testing, returned to vendor for repair, retested successfully

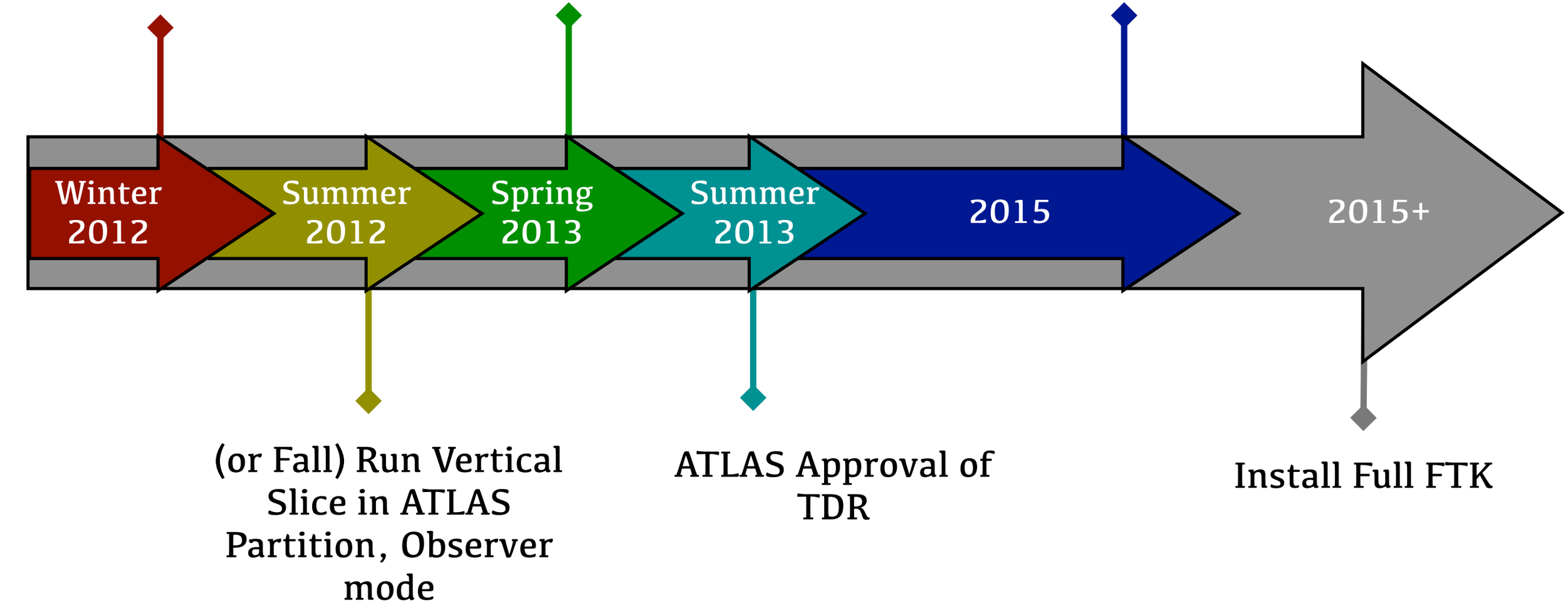




Vertical Slice



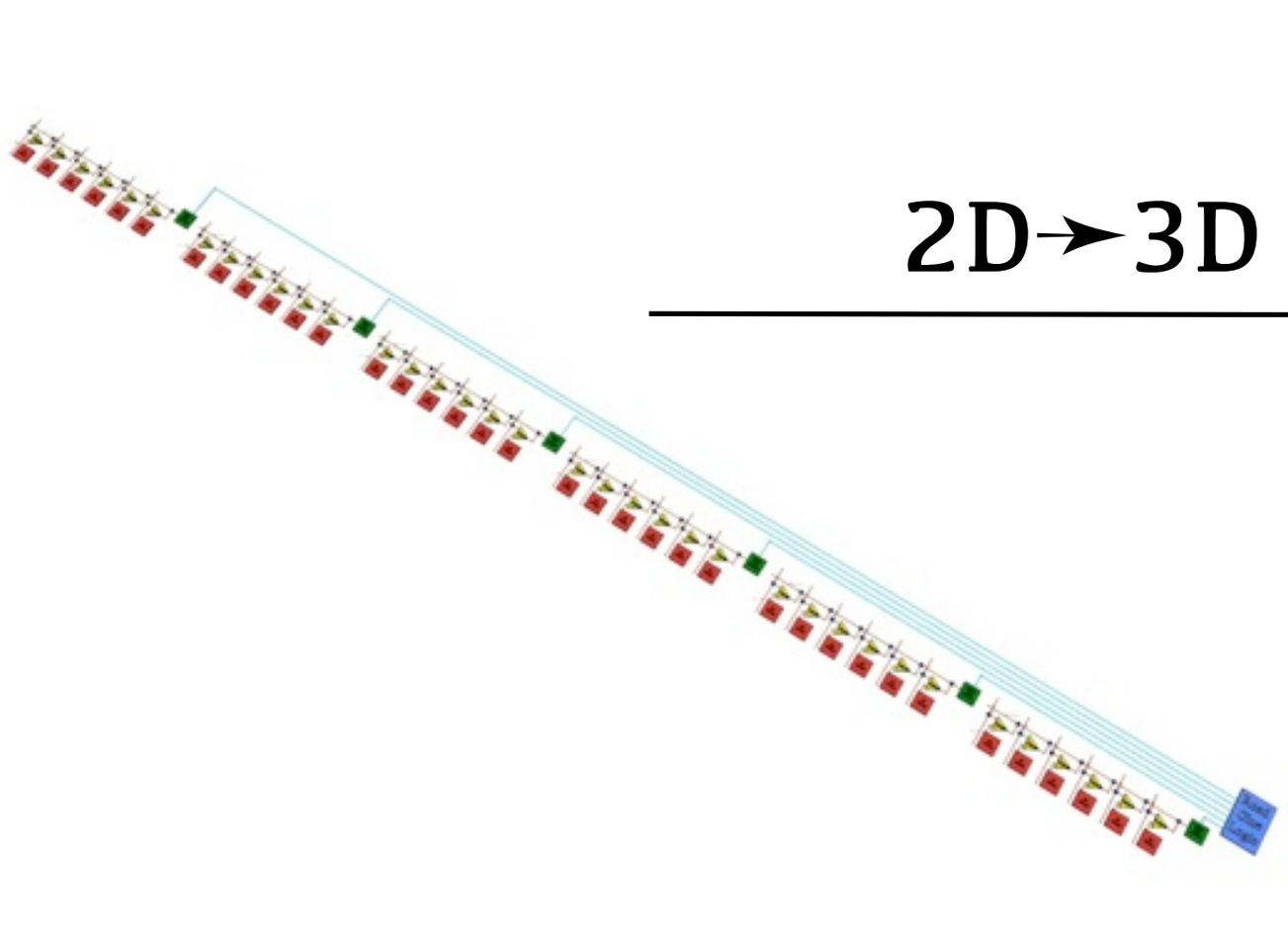
FTK Status and Plans



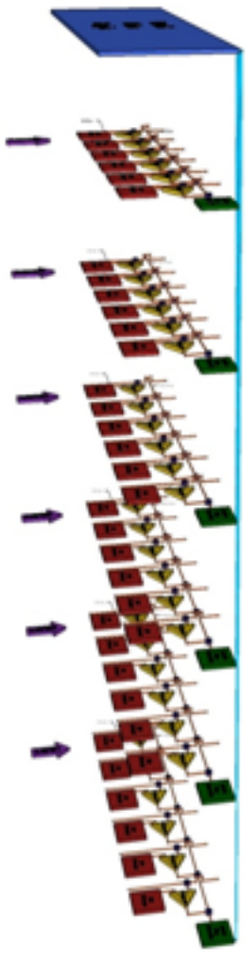
Beyond Phase 1

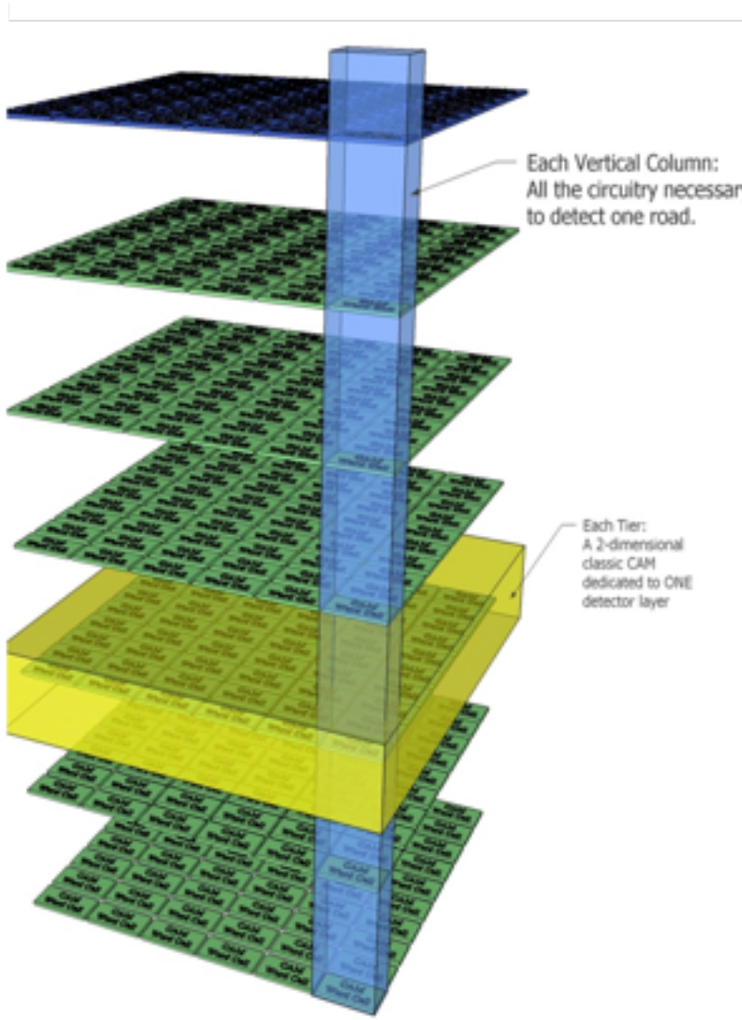
- Challenges of triggering only become harder at HL-LHC-Phase2(7e34)
- ATLAS considering 2 stage replacement for L1:
  - L0: ~5 μs latency, calo and muon trigger
  - L1: ~30 μs latency, do ROI based tracking
- FTK like system could be used in new L1
- Need much higher pattern density @ > 100 int/x-ing!
- AMChip04 near limit of conventional associative memory densities
- For SLHC need:
  - More speed (3x)
  - Higher pattern density (5x)

Going to 3D Silicon processing



2D➛3D





- Exploit nascent 3D silicon processing technology
- Physical detector layers⟷silicon layers
- Fast, high density solution: Exciting!

VIPRAM concept (developed at Fermilab):
http://hep.uchicago.edu/~thliu/projects/VIPRAM/TIPP2011_VIPRAM_Paper.V11.preprint.pdf

FTK Collaboration

- Italy
  - INFN
  - Bologna
  - Frascati
  - Milan
  - Pavia
  - Pisa

AM boards
Clustering Mezzanine
Vertical Slice

- US
  - Argonne
  - Chicago
  - Fermilab
  - Northern Illinois
  - Illinois

Data Formatter
Aux Card
Second Stage Board
FLIC crate

- Japan
  - Waseda

Clustering Mezzanine