Lawrence Berkeley National Laboratory

Report on TIPP 2011 3D-IC Satellite Meeting

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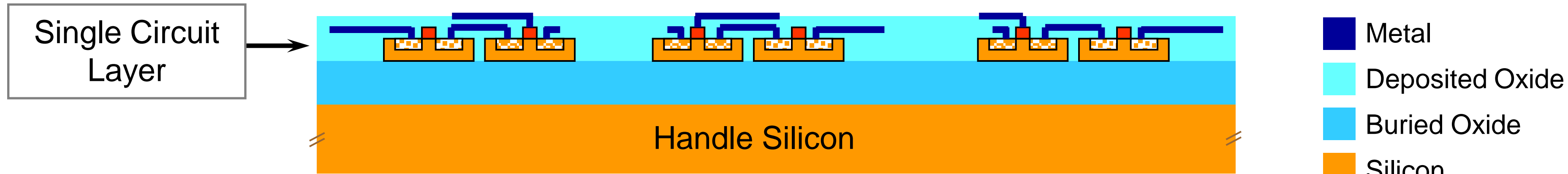
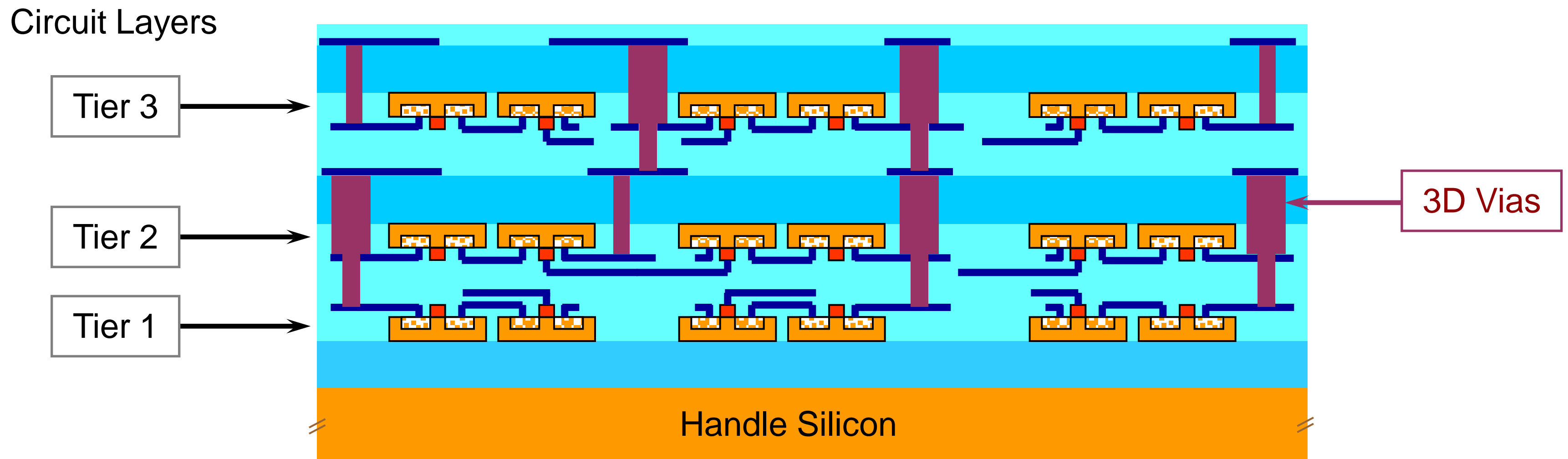
Key takeaways

- 3D-IC potentially a very valuable technology for detector improvement and we should continue to pursue it
- 3D-IC is conceptually simple, but in practice it is really, really hard
- Experiences thus far have been quite painful
- Until a foundry takes over, get ready for endless waits for parts and a tiresome blame game

2D versus 3D Circuits



2D Integrated Circuit Cross-Section



3D Integrated Circuit Cross-Section

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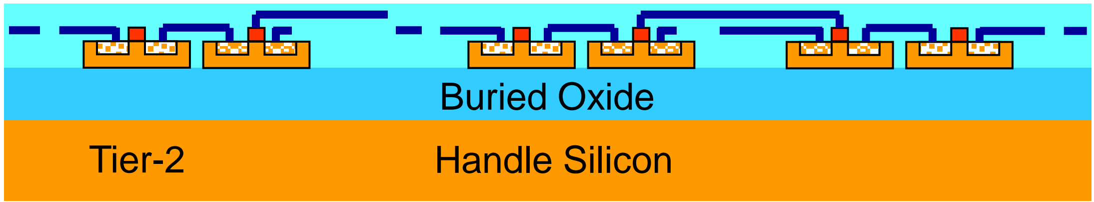
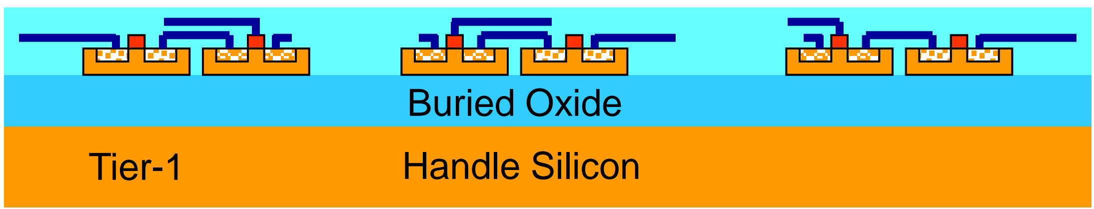
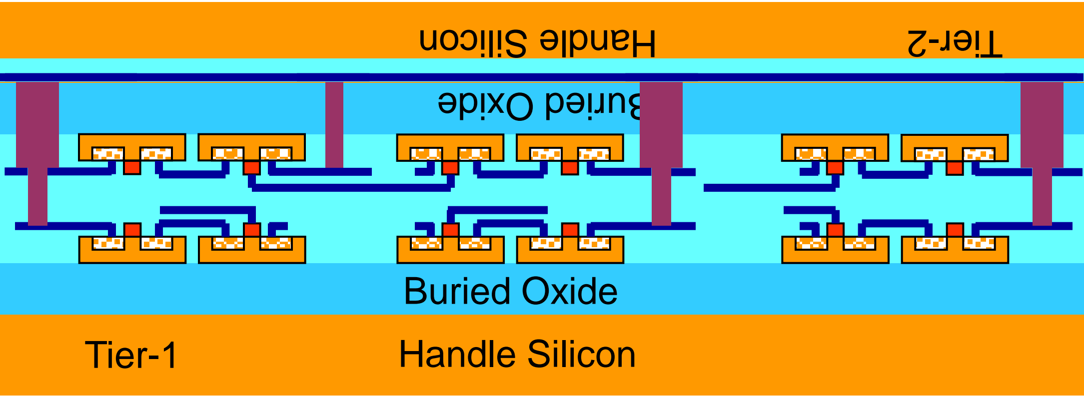
Tier2-to-Tier1 Alignment and Bonding





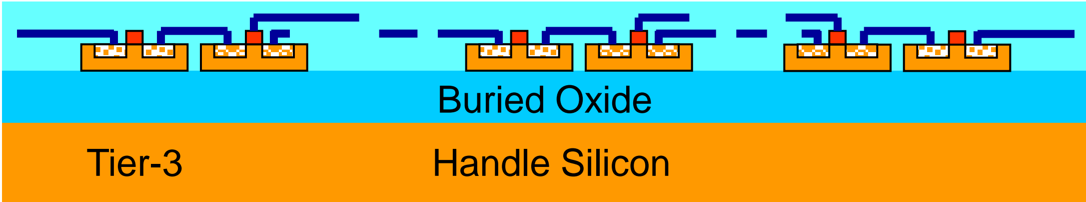
Metal
Deposited Oxide
Buried Oxide
Silicon

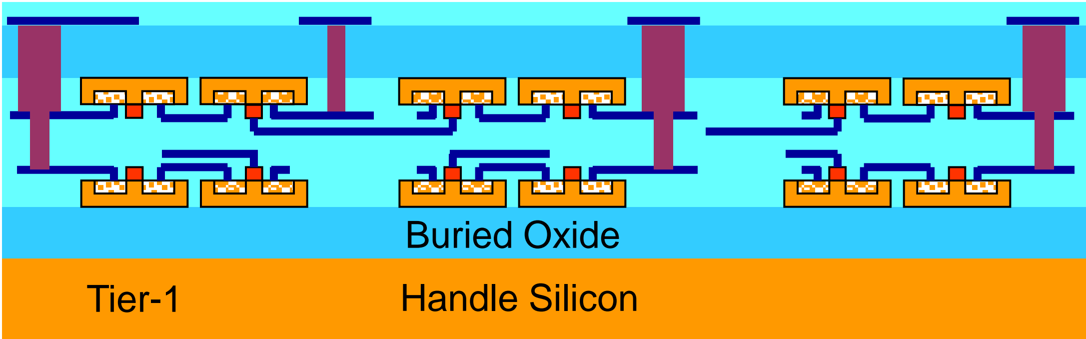
Tier2 Substrate Removal and Electrical Connection to Tier1



Tungsten
Metal
Deposited Oxide
Buried Oxide
Silicon

Tier3 Bonding and Alignment





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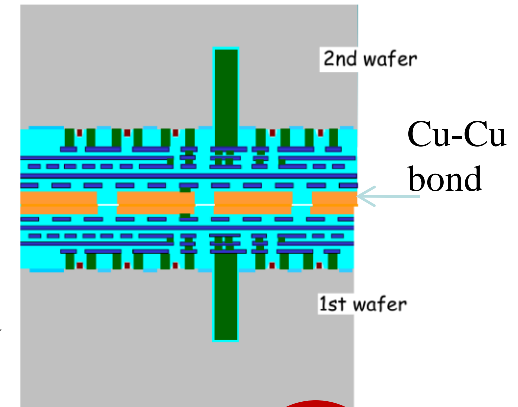
Tezzaron 3D MPW Run Experience

- In late 2008, consortium of 15 institutions formed to fabricated 3D integrated circuits using the Tezzaron/Chartered process.
  - Chartered uses a via middle process to add vias to 130nm CMOS process
  - Tezzaron performs 3D stacking using Cu-Cu thermo compression bonding

Assume identical wafers

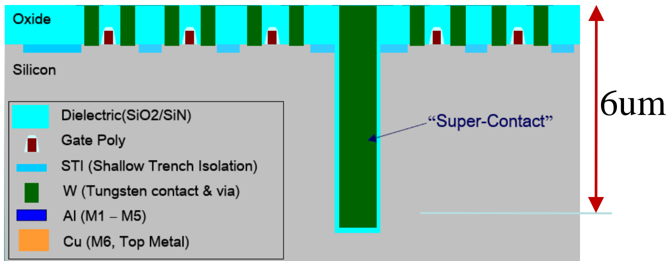
Flip 2nd wafer on top of second wafer

Bond 2nd wafer to 1st wafer using Cu-Cu thermocompression bond



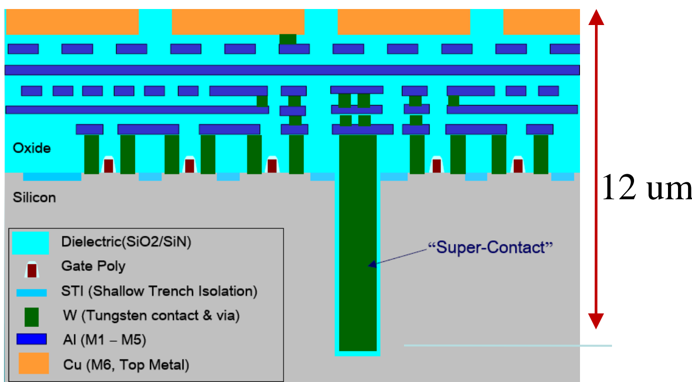
Cu-Cu bond

After FEOL fabricate 6 um super contact (via)



6um

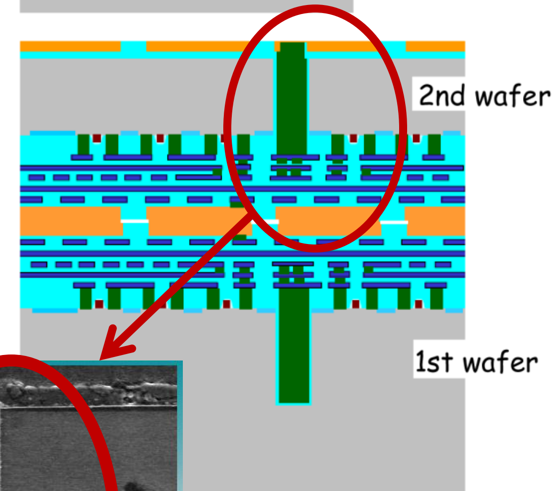
Complete BEOL processing



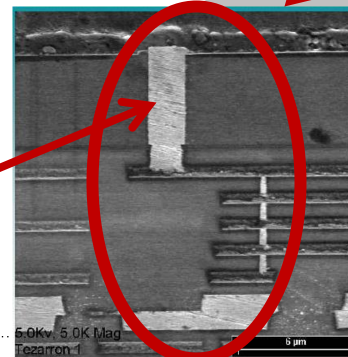
12 um

Thin 2nd wafer to about 12um to expose super via

Add metallization to back of 2nd wafer for bump or wire bond



TSV



Additional wafers can be stacked face to back on top of 2nd wafer

Possibilities offered by European Industry and Research Institutes

VTT
Frauenhofer IZM
IMEC
Frauenhofer EMFT
CEA LETI
(CMP)
CNM

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