Front-end ASICs for High Resolution Detectors

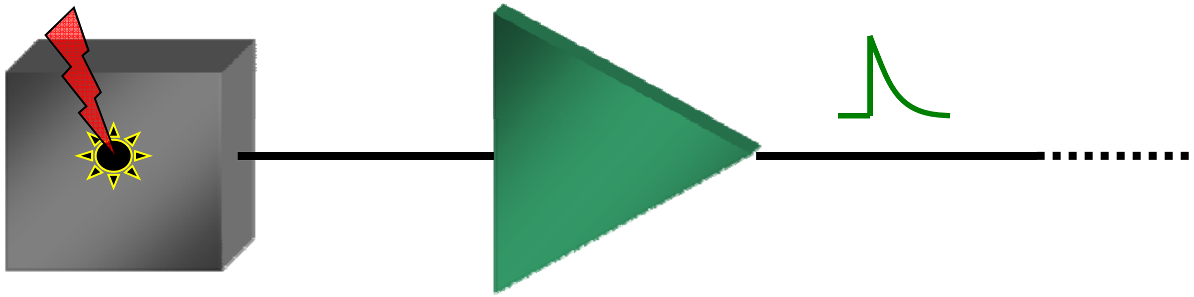
Gianluigi De Geronimo

Brookhaven National Laboratory, Upton, NY, USA

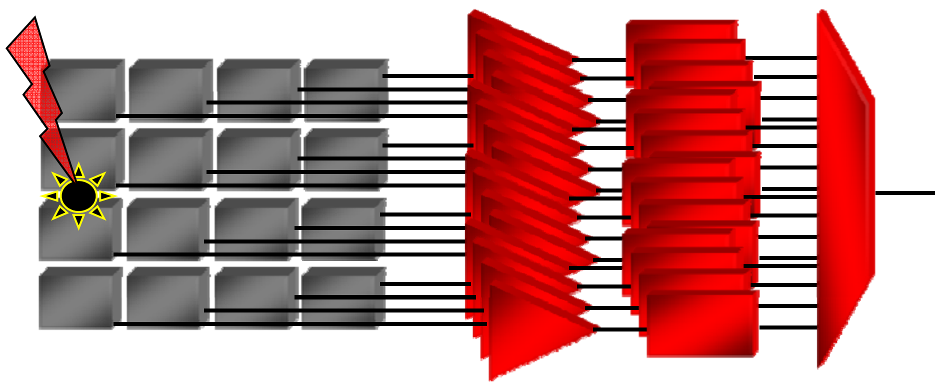
- State-of-the-art and design flow
- Examples of ASICs
- Peak detection
- ASIC in cryogenic environment
- Prospects for Germanium sensors

Motivation

Electronics for radiation detectors consists of low noise readout of signals generated in the sensor by ionizing radiation



Low density, low functionality ➔ discrete electronics



High density, high functionality ➔ ASICs

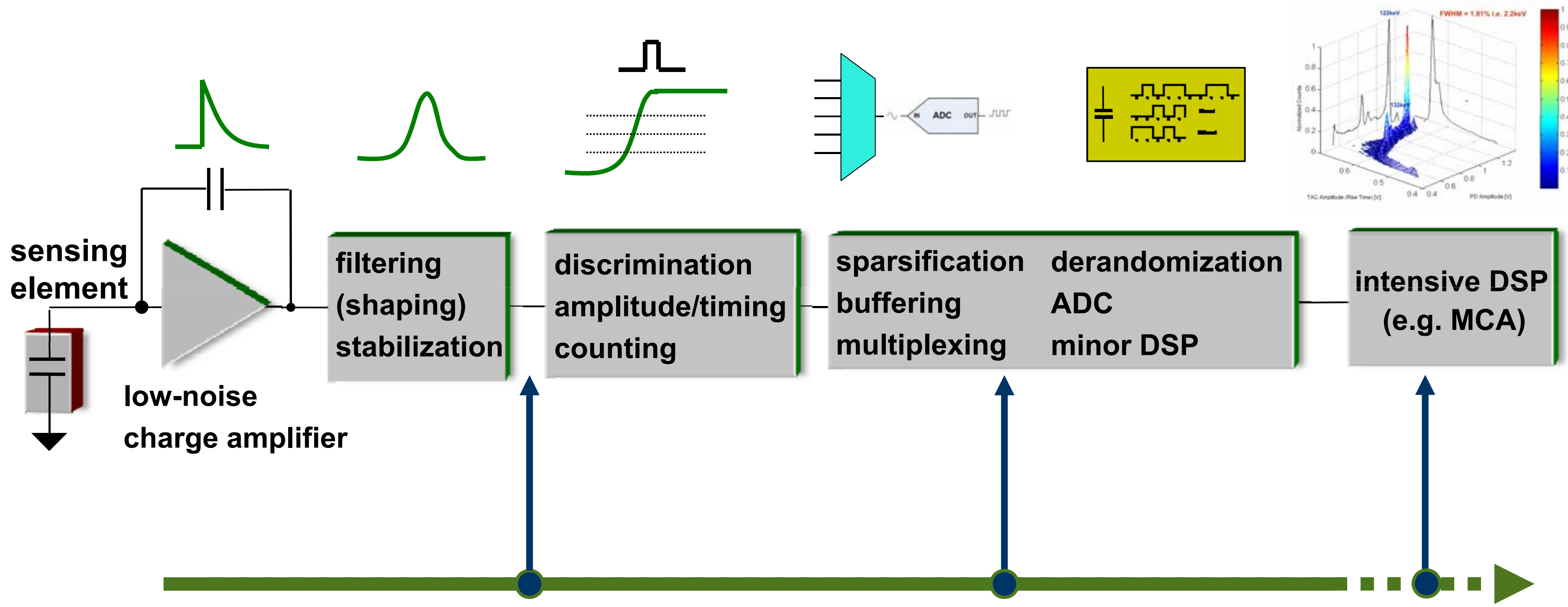
specifically designed,
not available off-the-shelf

Application
Specific
Integrated
Circuits

ASICs have enabled entirely new classes of radiation detectors to be constructed

State-of-the-Art

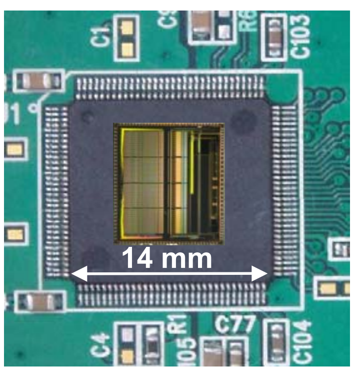
typical front-end electronics channel



year 2000
- 500 nm technology
- 16,000 transistors
- 16 channels
- analog

year 2010
- ~ 180 nm technology
- ~ 1M transistors
- ~ 100 channels
- analog and digital (*mixed-signal*)

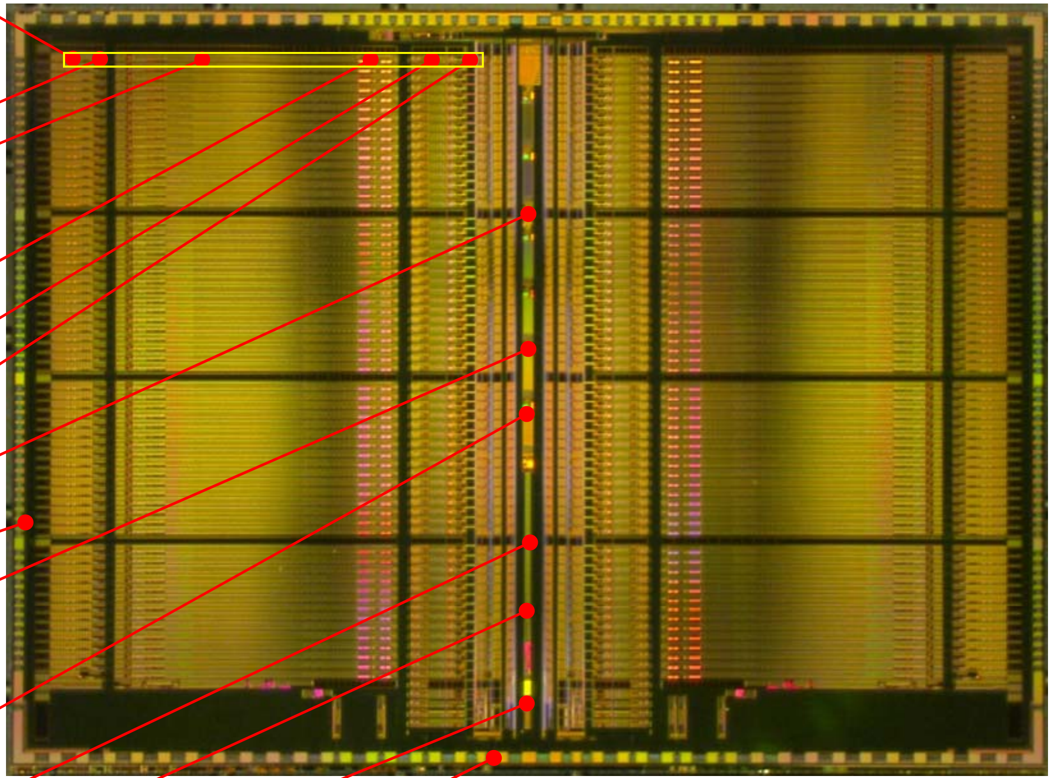
by 2013
- ≤ 130 nm technology
- >> 1M transistors
- >> 100 channels



(2007) - 64-channel ASIC for Neutron Detectors: charge amplifier, filter, peak detector, 6-bit ADC, 18-bit timestamp, FIFO, MUX, 1.5 mW/ch, 110 e^- rms

Subcircuits

- Low-noise, low-power **charge amplifiers**
  - gas, liquid, solid state detectors
  - capacitances **from 10 fF to 10 nF**
- Switched and continuous **adaptive reset**
- **High-order filters**, stabilizers, drivers
  - peak time / gain adjustment
- Single- and multi-level **discriminators**
- **Peak and time detectors**, derandomizers
- **Analog memories and multiplexers**
- **Counters** and digital memories
- Configuration registers
- ESD protections
- **Test pulse generators**
- **Analog-to-digital** converters
- **Digital-to-analog** converters
- Precision **band-gap references**
- **Temperature sensors**
- Readout control logic
- Low-voltage **differential signaling**
- **Current-mode** analog and digital interface

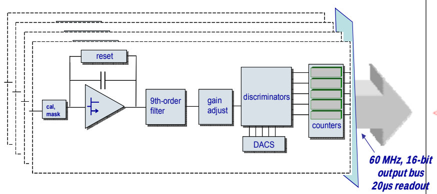


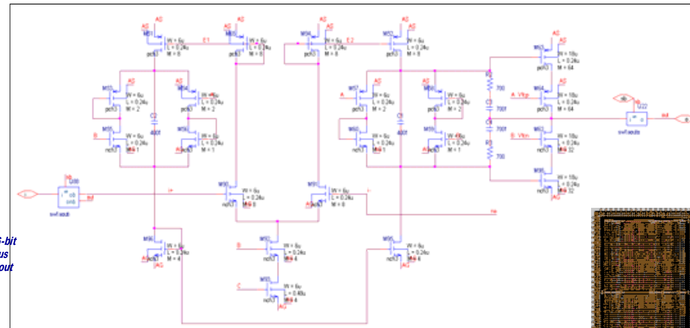
(2008)

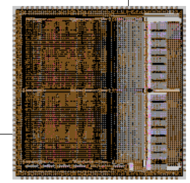
ASIC for 3D Position Sensitive Detectors

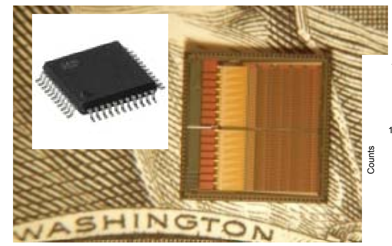
- **130 channels**
- **2.5 mW/channel**
- **13 x 9 mm²**
- **320,000 transistors**

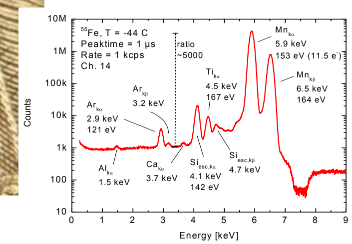
ASIC Design Flow











design phase	system level design	transistor level design	masks layout	fabrication	tests
months	~ 2	~ 6	~ 2	~ 3	~ 2

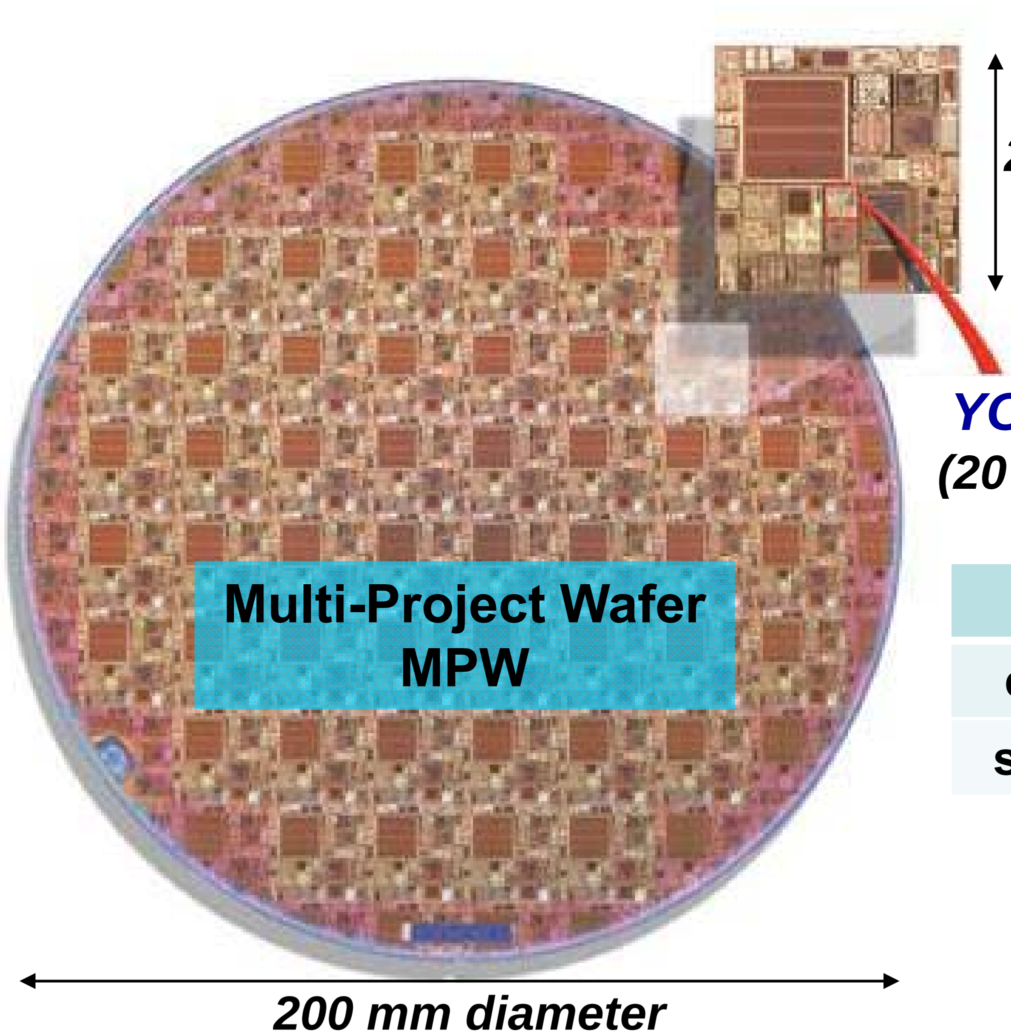
revision cycles

From concept to ready-for-production:
1 - 2 rev. cycles, 2 - 3 years (depending on complexity)

Progressive increase in functionality and complexity require more resources, more expertise, and/or longer development time

ASIC Fabrication : Prototyping

Major foundries accept designs from different customers (MPW)



YOUR ASIC is here

(20 mm², ~ 60,000 transistors)

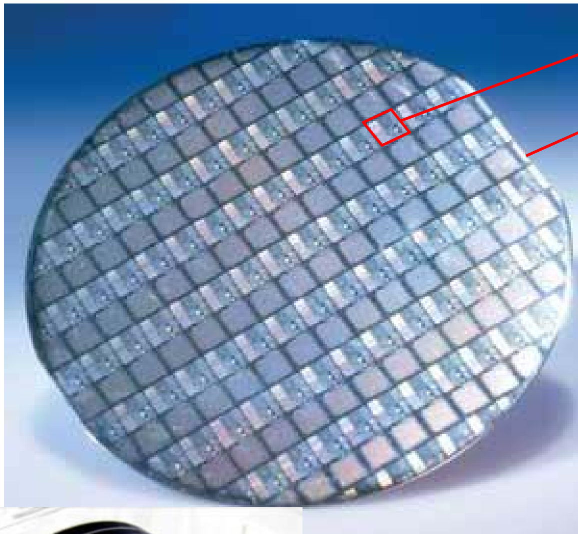
	MPW	DEDICATED
cost [$]	10k to 100k	100k to 700k
samples	tens	thousands

↓

ideal for **prototyping**
and **low volume**

ASIC Fabrication : Production

Major foundries accept the purchase of a dedicated run



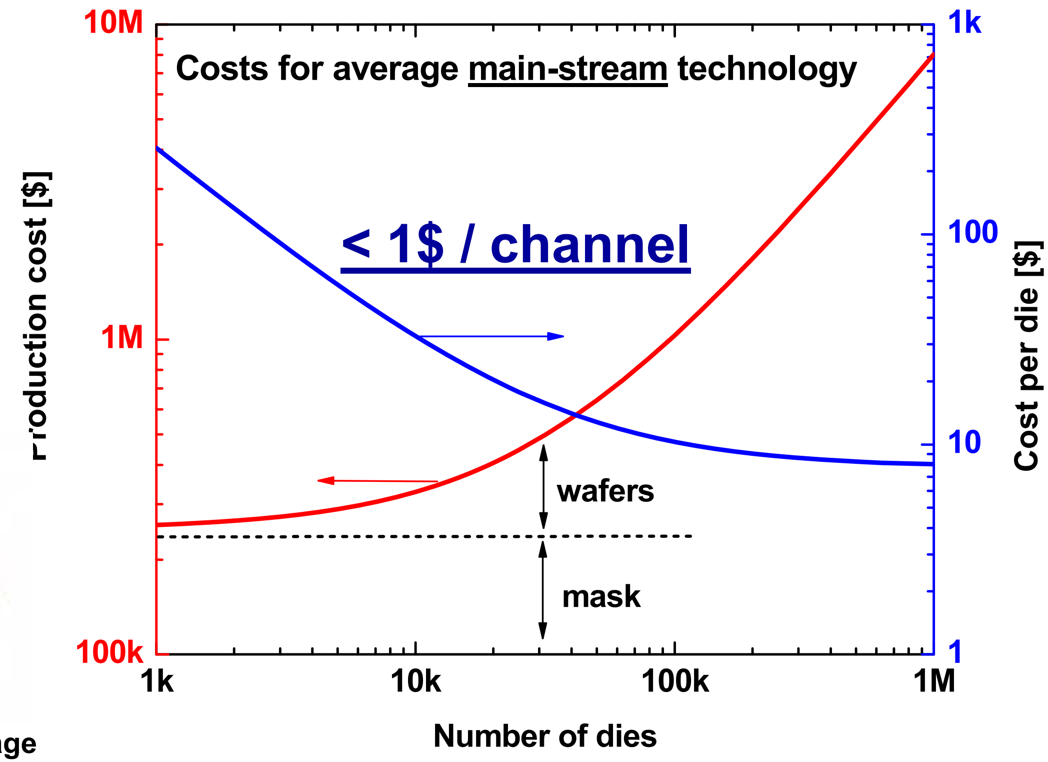
4-10 chips in a ~20x20 mm^2 reticle

~ 55 reticles per 8" wafer

	cost [$]
mask	100k to 700k
each wafer	1k to 10k

Packaging ~ $ 1.75 / die

14 x 20 QFP package
(cavity 11x13 mm²)



Main Stream Technologies

2010 MPW fabrication schedule

- from MOSIS Service (mosis.org)

Typical applications

- CMOS **≥130nm**: <GHz **analog, mixed-signal**
- CMOS **<130nm**: >GHz analog, digital
- **SiGe** (HBT): >>GHz analog
- **SOI**: >>GHz analog, high-density digital
- **HV**: >>high-voltage (>30V)

All of these are **main stream**
- available at MPW services
- used for prototyping

Technologies with **highest schedule** are expected to be **available for several years**.

Technologies with **smaller feature size** require **lower voltage** and are **more expensive**

Low voltage has impact on
- **design complexity**
- **dynamic range (or area ...)**

Year	Technology node (nm)
2009	40
2008	45
2006	65
2002	90
2000	130
1999	180
1998	250
1995	350

TSMC — Customer Submission Date

Technology		Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
CLN40/CMN40	40 nm **0.9V**			22	19	17	21	19	16	20	18	15	
CLN45/CMN45	45 nm			22	19	17	21	19	16	20	18	15	
CLN65/CMN65	65 nm **1V**	4 19	8 22	8 29	12 26	10 24	7 28	12 26	9 23	7 27	11 25	8 22	6
CLN90/CMN90	90 nm	4	8	8	5	3	1	6	2 30		4	1 29	
CL013/CM013	0.13 µm **1.2V**	19	8 22	8 29	12 19	3 17	1 28	26	23	27	25	22	
CL013LP	0.13 µm	19	8 22	8 29	12 19	3 17	1 28	26	23	27	25	22	
CL013LV	0.13 µm	19	8 22	8 29	12 19	3 17	1 28	26	23	27	25	22	
CL018/CM018	0.18 µm **1.8V**	4 19	8 16	8 15 22	5 19	3 10 17	7 14 21	6 19	2 9 16 30	7 20	4 18	1 8 15 29	6
CL018HV HV	0.18 µm	4		8		3		6	30			1	
CL018LP	0.18 µm	4 19		8 15	19	3	14	6 19	30	7	18	1	6
CL018LV	0.18 µm	4 19	8 16	8 22	5 19	3 10 17	7 21	6 19	2 9 16 30	7 20	4 18	1 8 15 29	6
CL025/CM025	0.25 µm **2.5V**	4 19	22	29		10	14	6 19	2 30	20	4	1 15 29	
CL035/CM035	0.35 µm **3.3V**	4		15	26		21		16		18		
CL035HV_BCD	0.35 µm				26				16				
CL035HV_DDD HV	0.35 µm	4 (1)		15 (2)	26 (1)		21 (2)		16 (1)		18 (2)		

IBM — Customer Submission Date

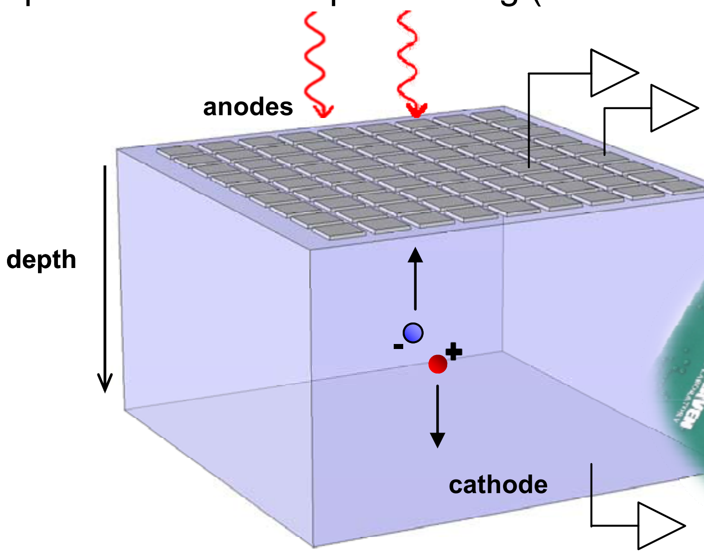
Technology		Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
32SOI [1] SOI	32 nm **0.9V**									27			
12SOI [1] SOI	45 nm							12					
10LPE [1]	65 nm **1V**	19		15					9				
10SF [1]	65 nm		1				21						
9LP	90 nm		22			24				27			6
8HP	0.13 µm **1.2V**		16			17				13			6
8RF [2]	0.13 µm		16			10			9			8	
8WL SiGe	0.13 µm		16			24				20			13
7HV [1] HV	0.18 µm **1.8V**					3				13		29	
7RF	0.18 µm		16		19		14		16		11		6
7RFSOI	0.18 µm	11		15			7		16		11		13
7WL SiGe	0.18 µm	19		15		3		12		7		8	
6WL [1] SiGe	0.25 µm **2.5V**	19			5			12			4		
5HPE	0.35 µm **3.3V**		1		19			6				1	
5PAE	0.35 µm	19			12						11		

Year	nm
2010	32
	45
	65
	90
	130
	180
	250
1995	350

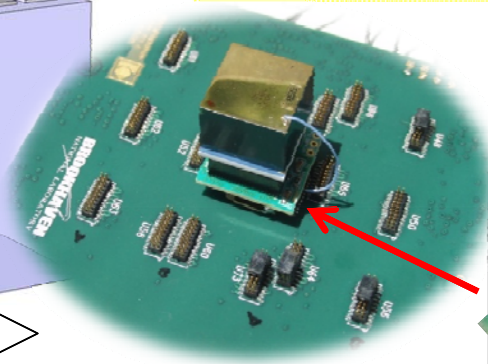
Some Examples

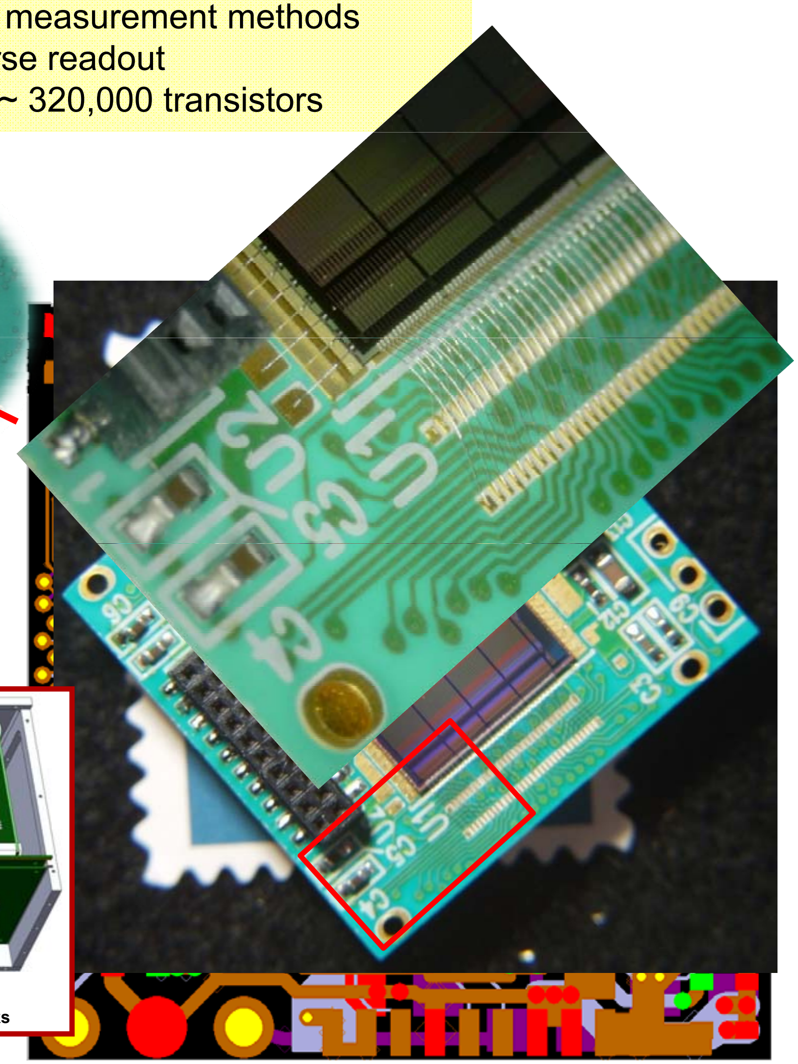
ASIC for 3D Position Sensitive Detectors (H3D)

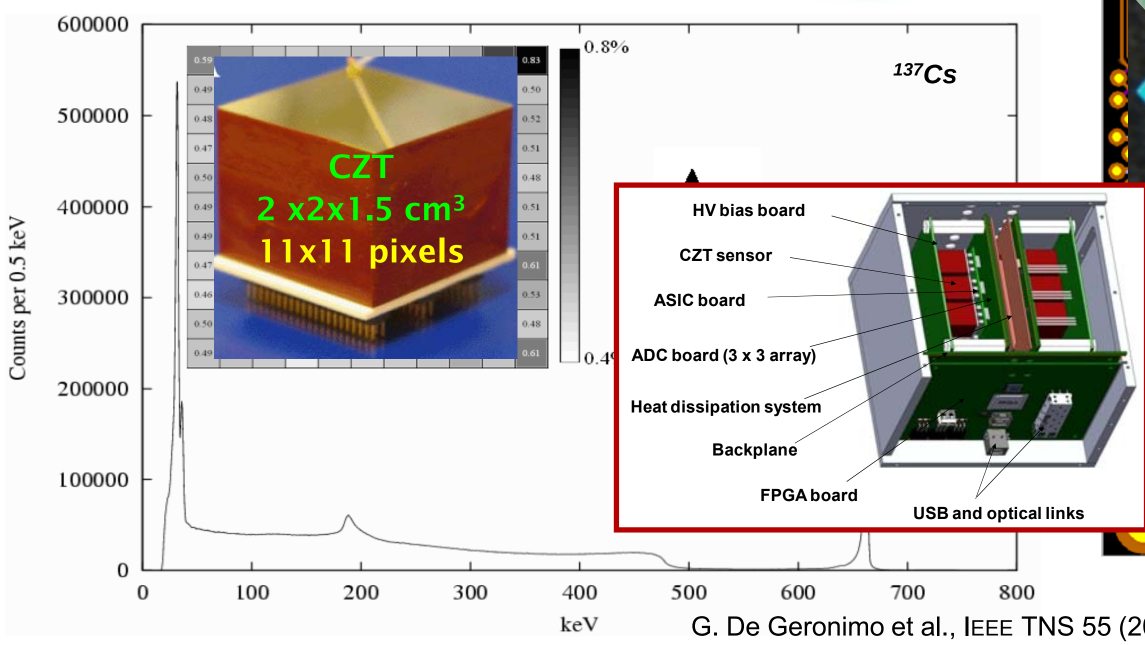
3D position sensitive detectors combine small-pixel effect with depth sensing (solid-state TPC)



- 130 channels - mixed signal
- low-noise anodes and cathode amplification
- **energy (sub-100 e$^-$) and timing (sub-ns)**
- multiple timing measurement methods
- advanced sparse readout
- ~ 2.5 mW/ch., ~ 320,000 transistors

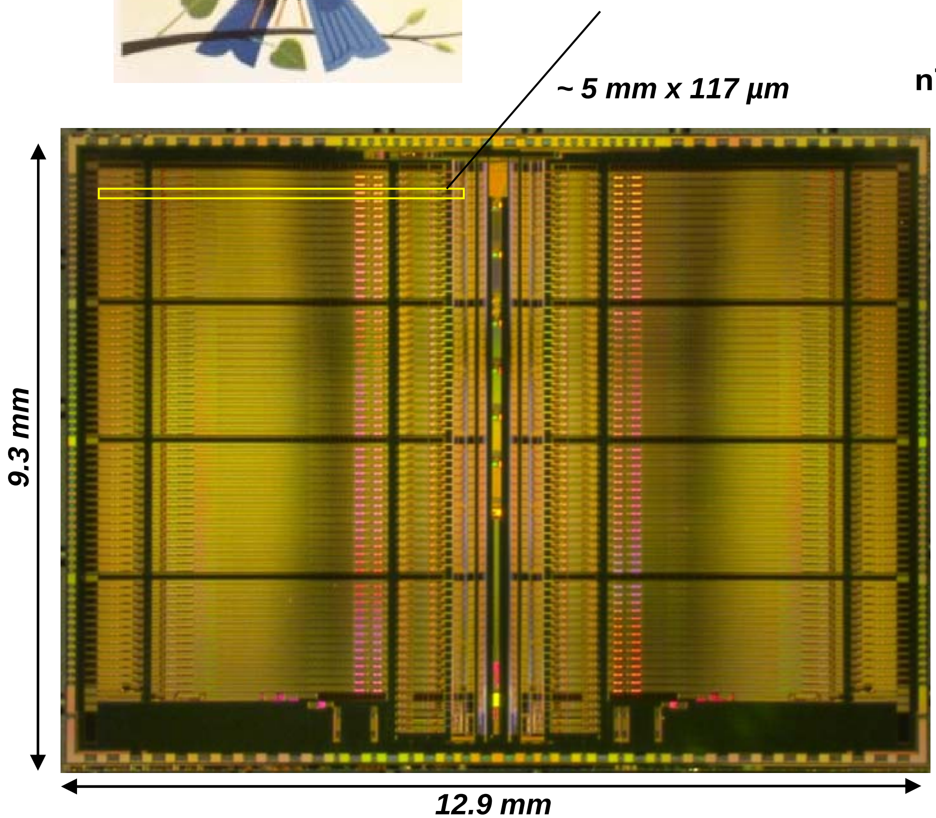


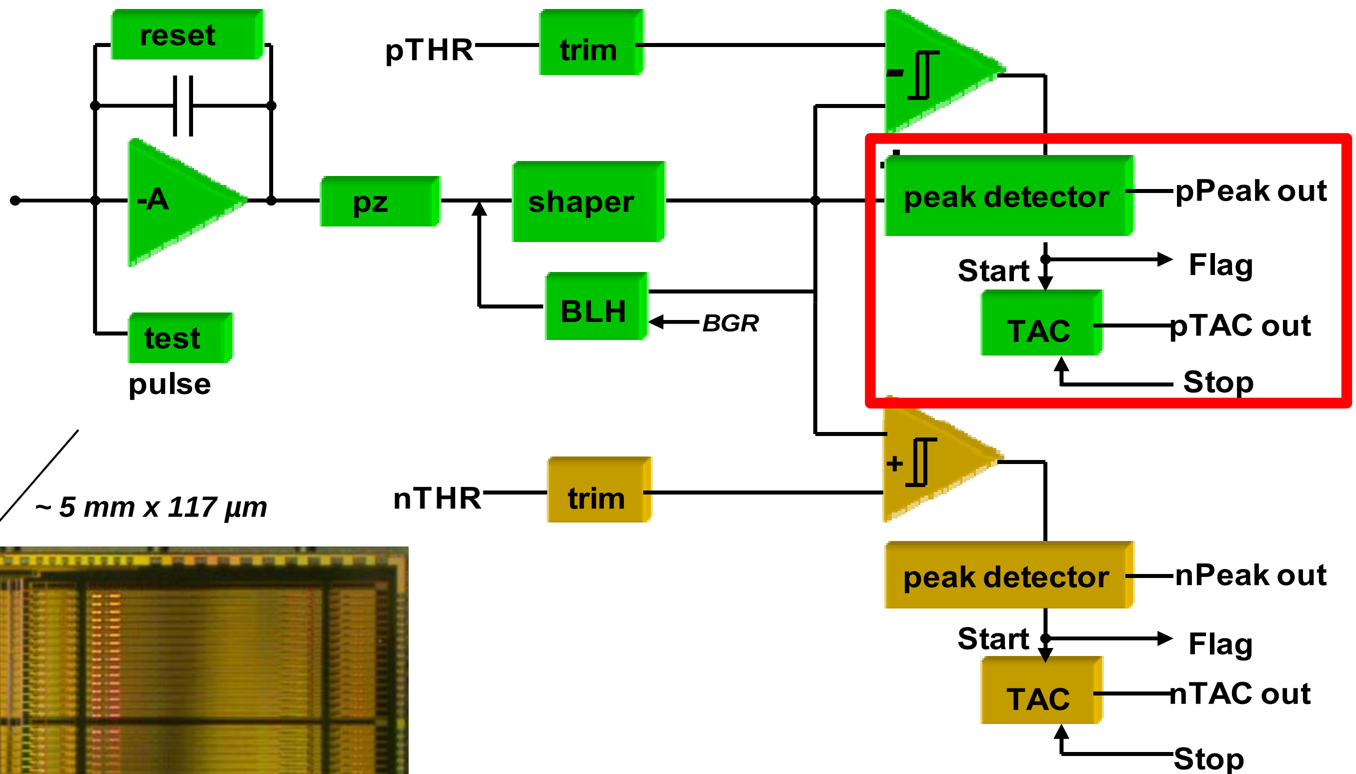




G. De Geronimo et al., IEEE TNS 55 (2008), collaboration with Michigan University, DHS, and DoD

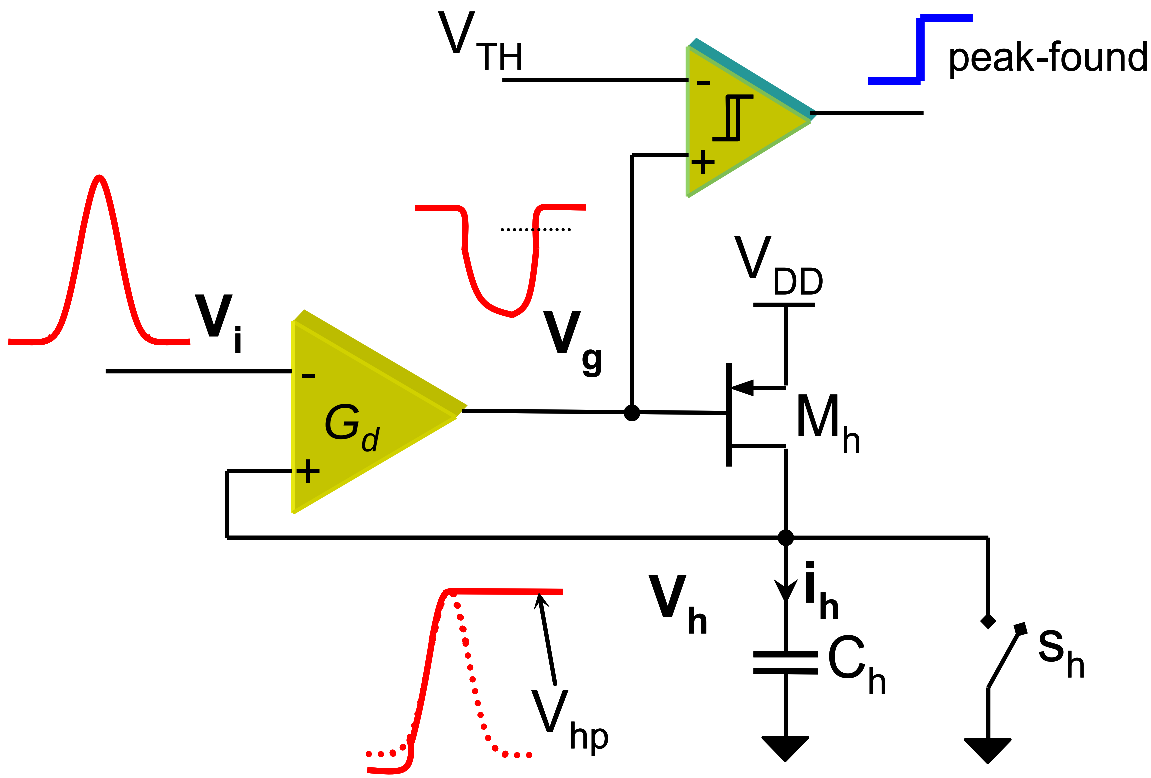
H3D Channel Architecture





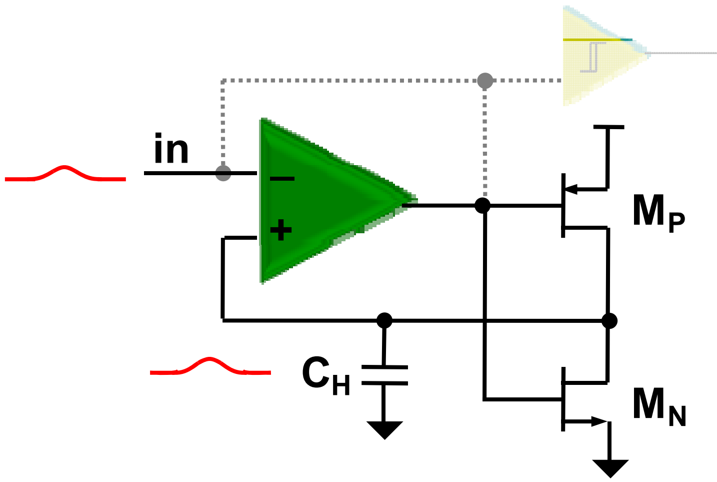
- Optimized for 3 pF input capacitance, 2.3 mW
- Adaptive continuous reset (up to 50 nA)
- 5^{th} order complex shaper
- Peaktime: 0.25, 0.5, 1, 1.5, 2, 3, 6 and 12 μs
- Gain: ≈ 20 & 60 mV/fC (3 MeV & 1 MeV in CZT)
- Multi-phase peak- and time-detector
- Low hysteresis discriminators (5-bit trim)

Peak Detector - Classical Configuration



- detects and holds peak without external trigger
- provides accurate timing signal (peak found, z-cross on derivative)
- low accuracy (op-amp offset, CMRR)
- poor drive capability

Peak Detector - Multiphase

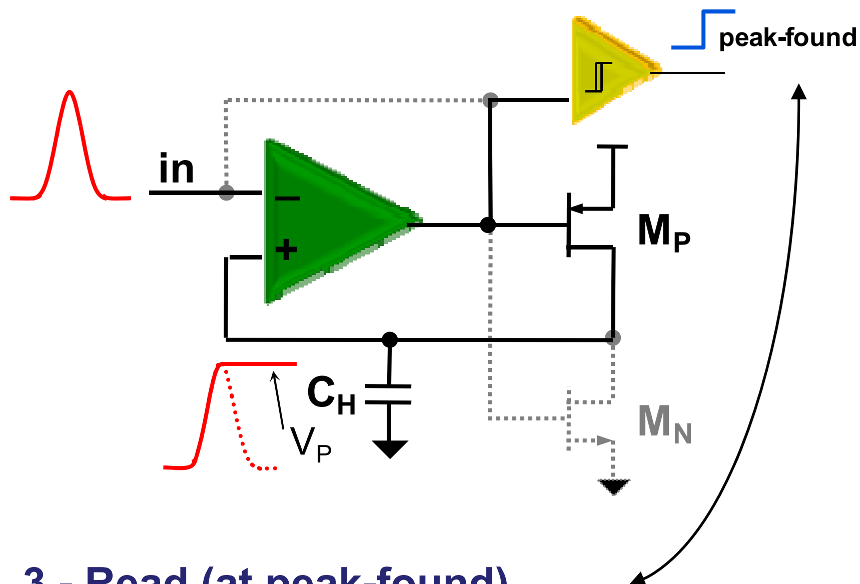


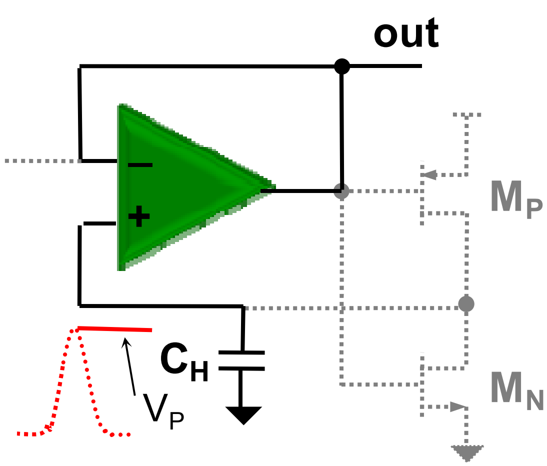
1 - Track (< threshold)

- Analog output is tracked at hold capacitor
- M_P and M_N are both enabled

2 - Peak-detect (> threshold)

- Pulse is tracked and peak is held
- Only M_P is enabled
- Comparator is used as peak-found



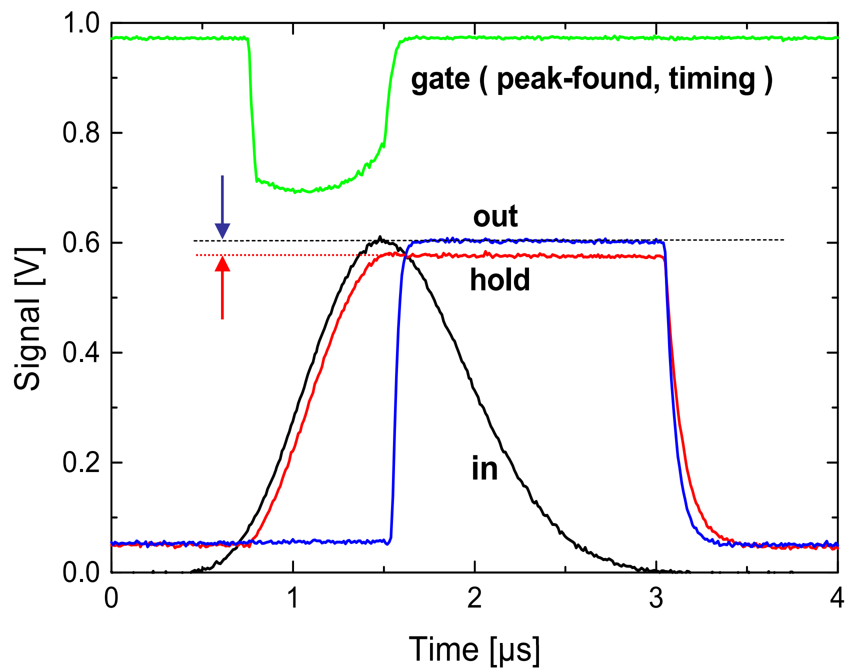


3 - Read (at peak-found)

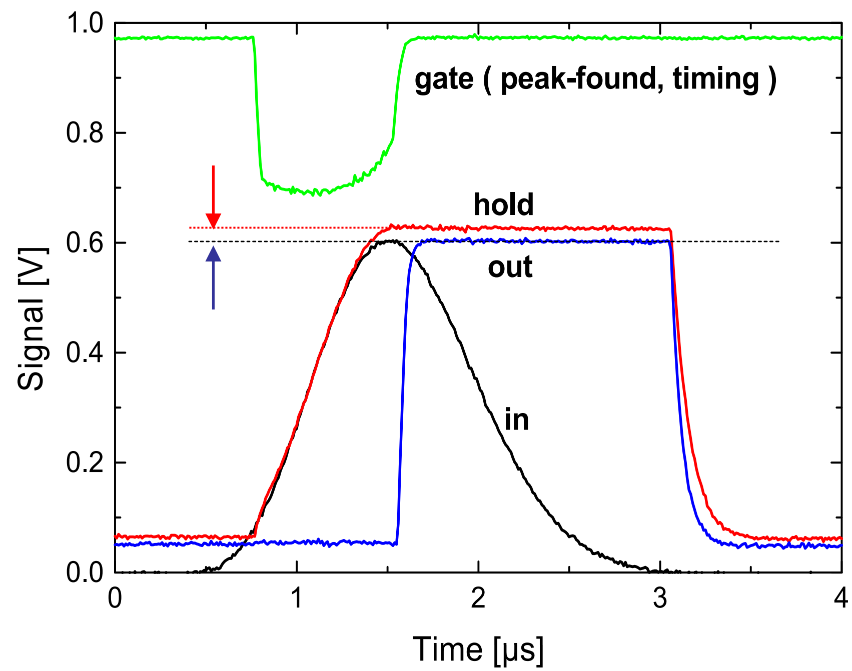
- Amplifier re-configured as buffer
- High drive capability
- Amplifier offsets is canceled
- Enables rail-to-rail operation
- Accurate timing
- Some pile-up rejection

Peak Detector - Multiphase

Chip 1 – negative offset

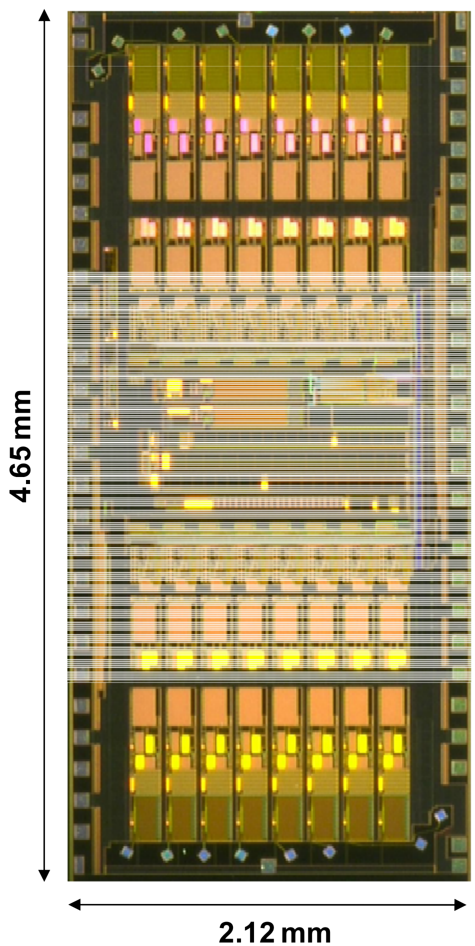


Chip 2 – positive offset

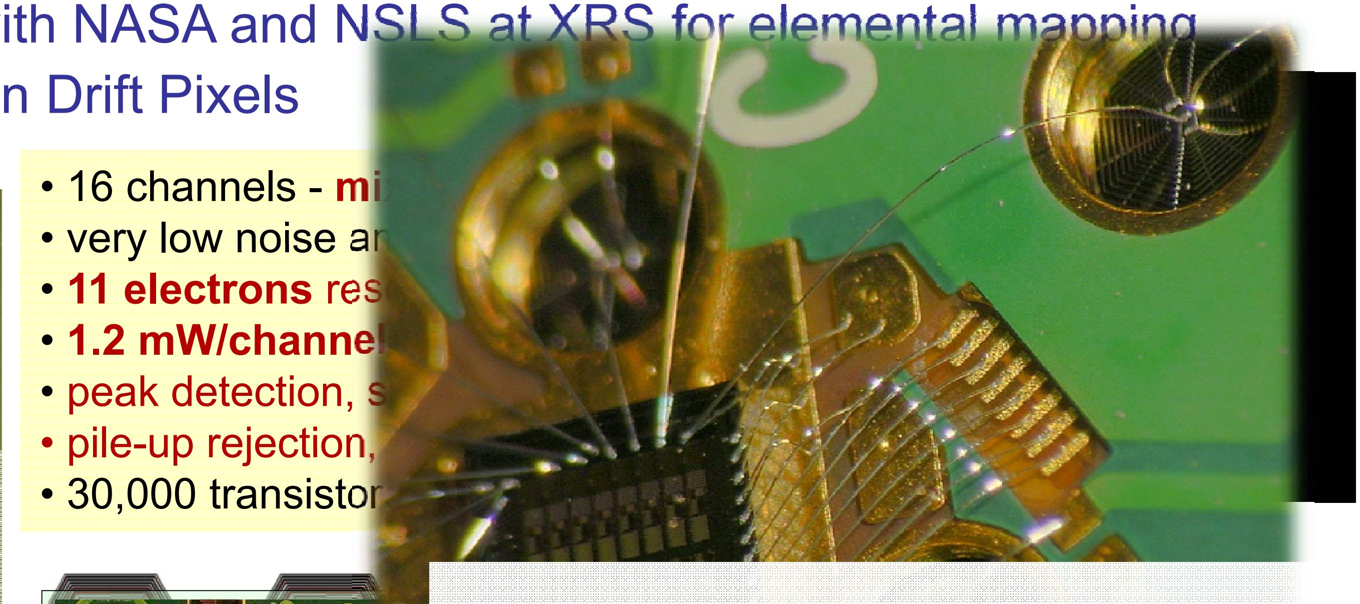


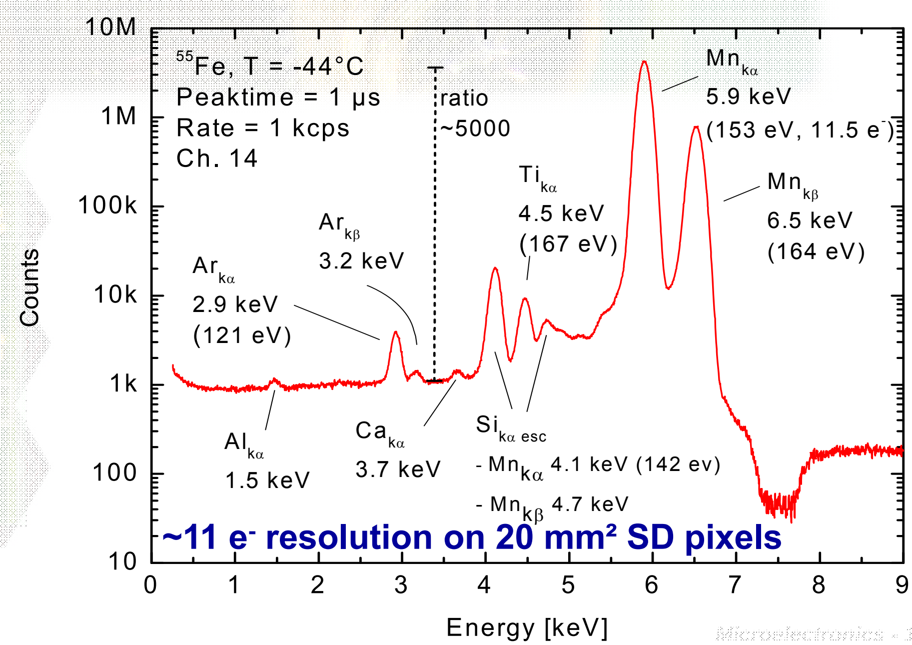
ASIC for High-Resolution X-ray Spectroscopy

- Collaboration with NASA and NSLS at XRS for elemental mapping
- Based on Silicon Drift Pixels



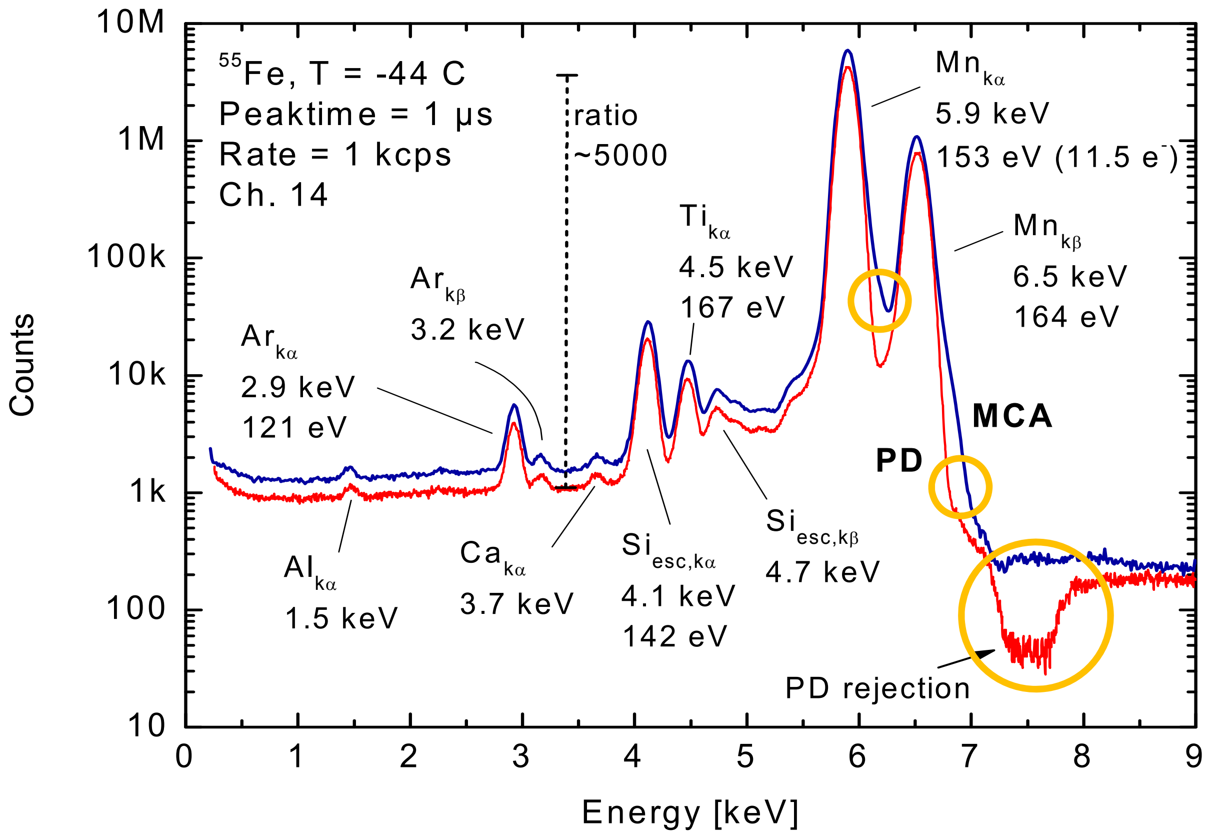
- 16 channels - **mi**
- very low noise ar
- **11 electrons** res
- **1.2 mW/channel**
- peak detection, s
- pile-up rejection,
- 30,000 transistor

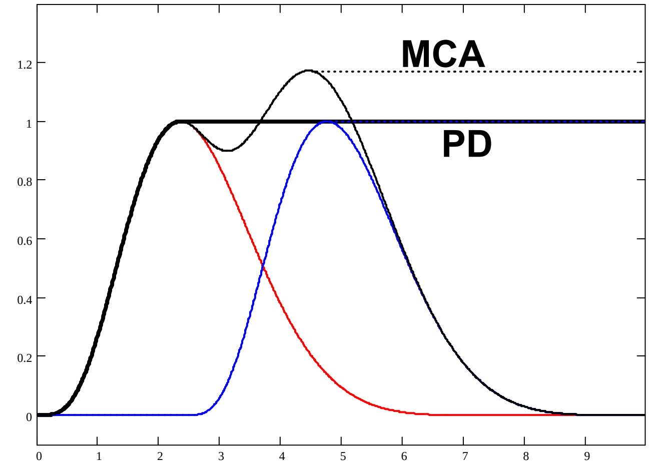


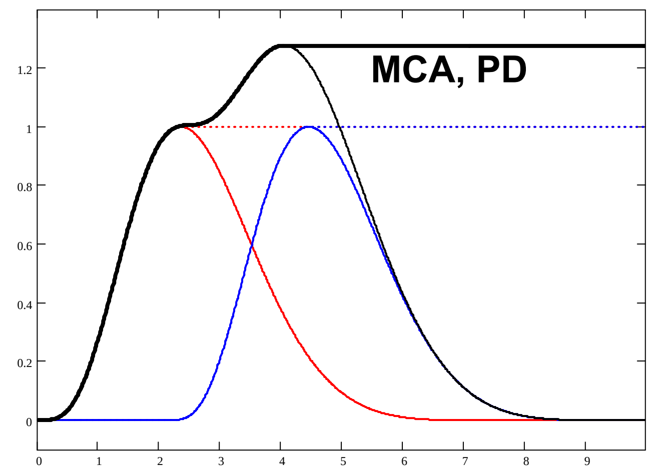


G. De Geronimo et al., IEEE TNS 55 (2008), collaboration with NASA

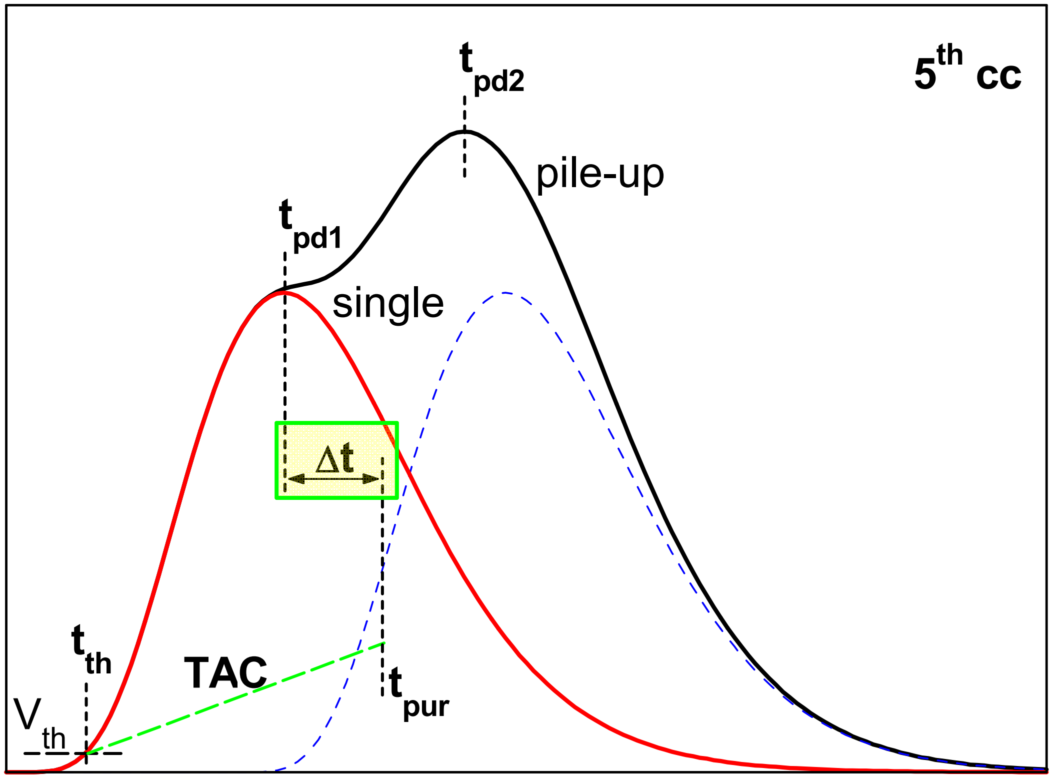
Peak Detector vs Commercial MCA

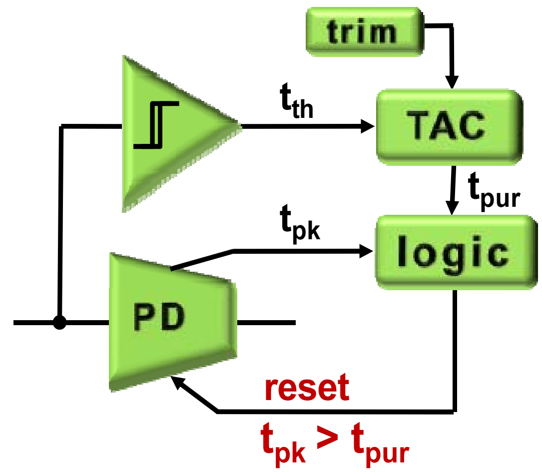


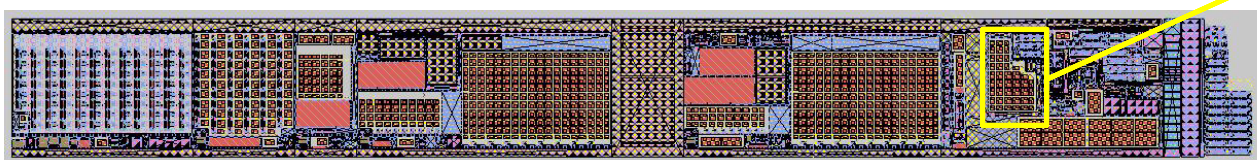




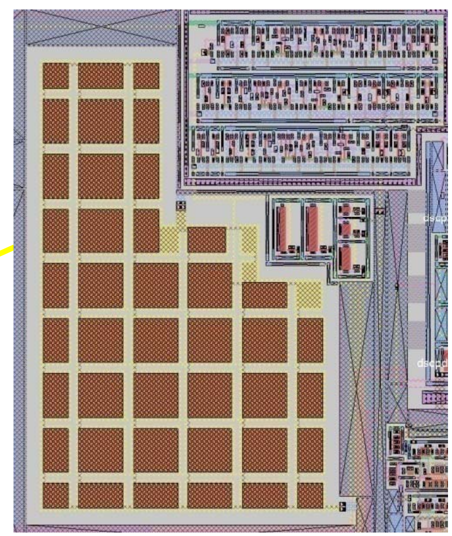
Pile-up Rejector (PUR)





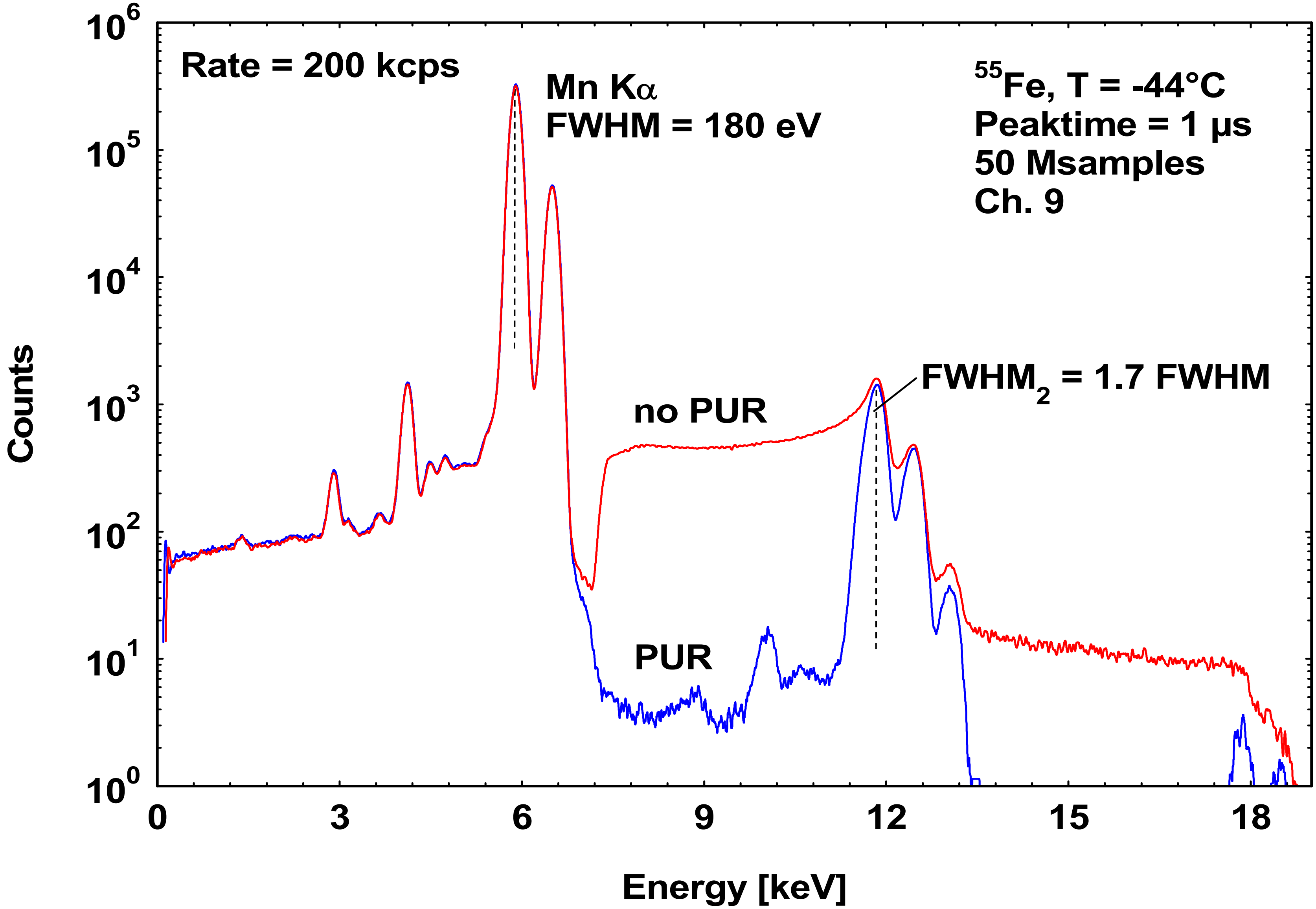


channel 1700 x 200 μm^2



90 x 100 μm^2, < 1 μW at 200 kcps

High-Rate Spectral Measurement with PUR



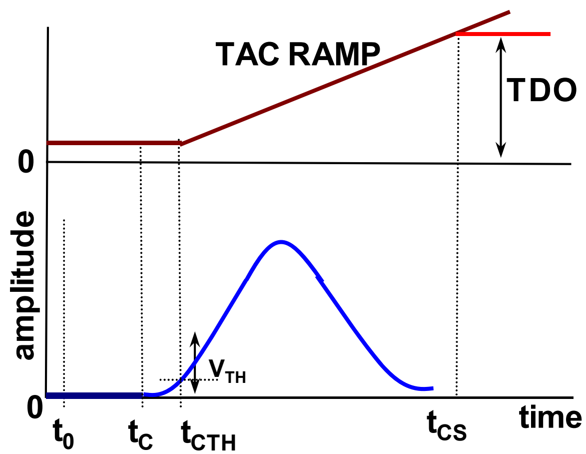
$$FWHM_2 \approx \sqrt{2 \cdot FWHM_{stat}^2 + FWHM_{elec}^2 + FWHM_{2,pileup}^2}$$

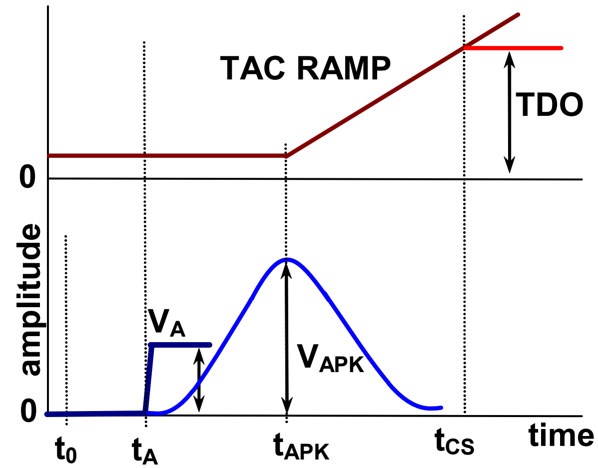
← asymm.

Peak Detector - Timing Function

Compare **timing at threshold crossing** with **timing at peak**

Threshold crossing | **Peak detection**





$$\sigma_t \approx \frac{ENC}{Q \left.\frac{ds}{dt}\right|_{@\,threshold}}$$

output slope normalized to unit charge

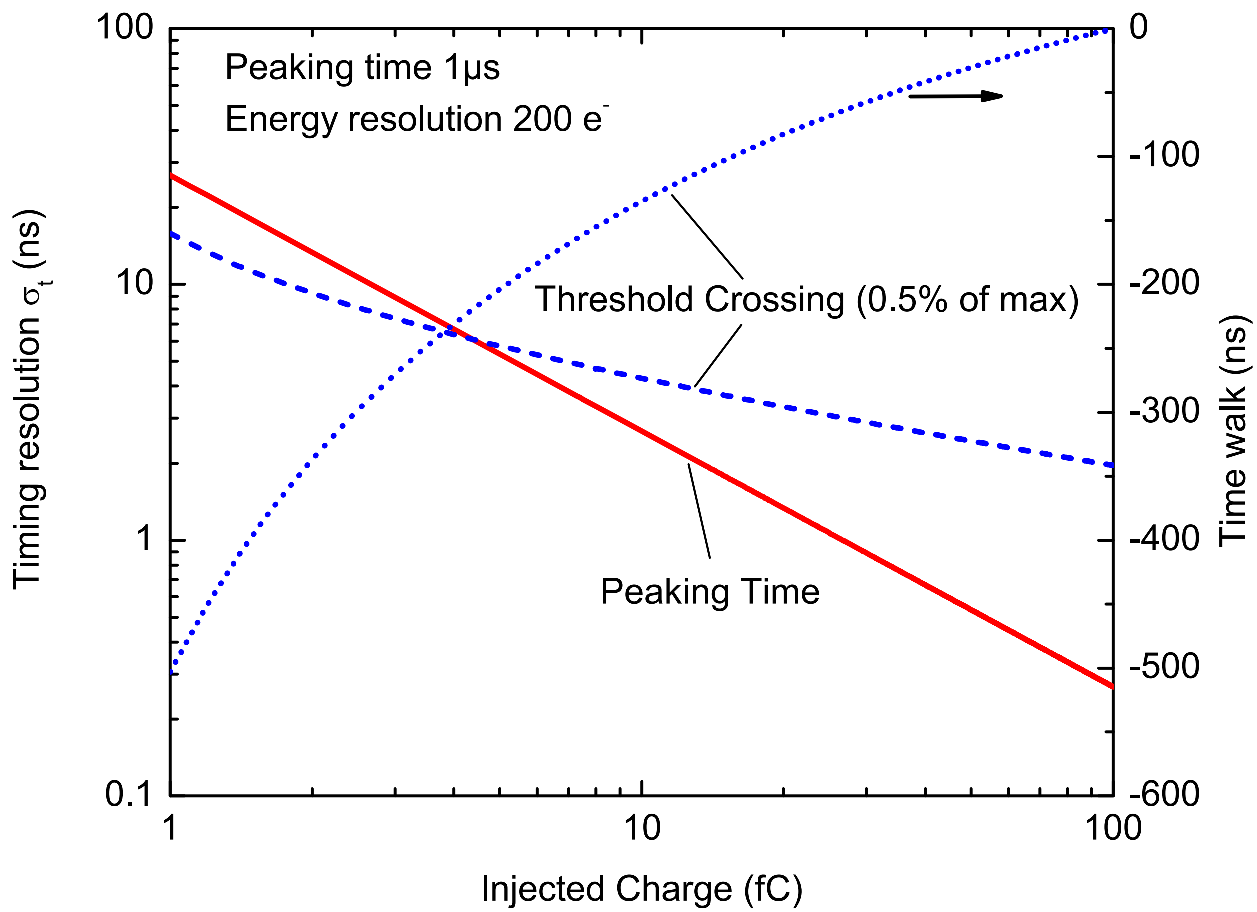
$$\sigma_t \approx \frac{ENC \cdot \tau_p \lambda_p}{Q\ \rho_p}$$

Time-walk strongly dependent on amplitude

Time-walk almost independent of amplitude (equivalent to zero crossing on differential)

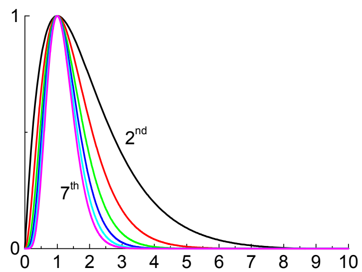
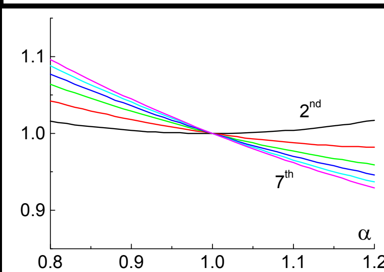
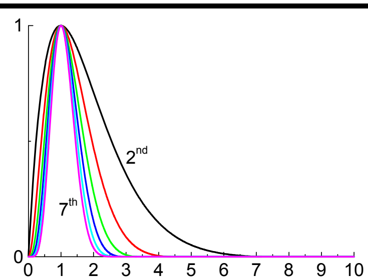
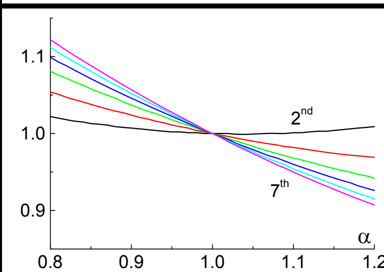
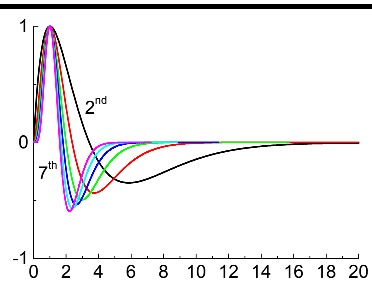
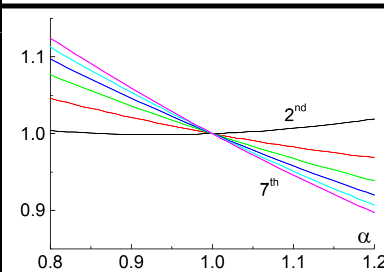
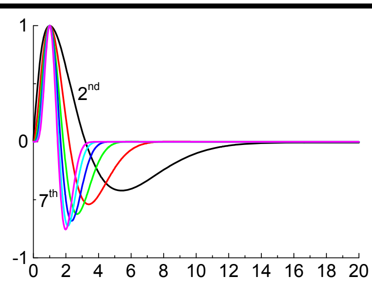
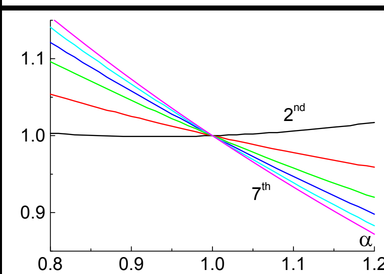
Peak Detector - Timing Function

Compare **timing at threshold crossing** with **timing at peak**

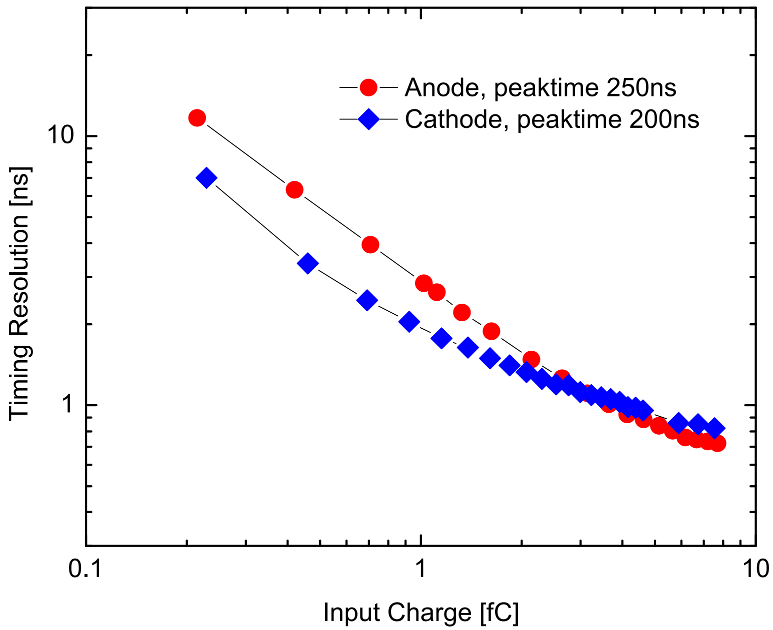


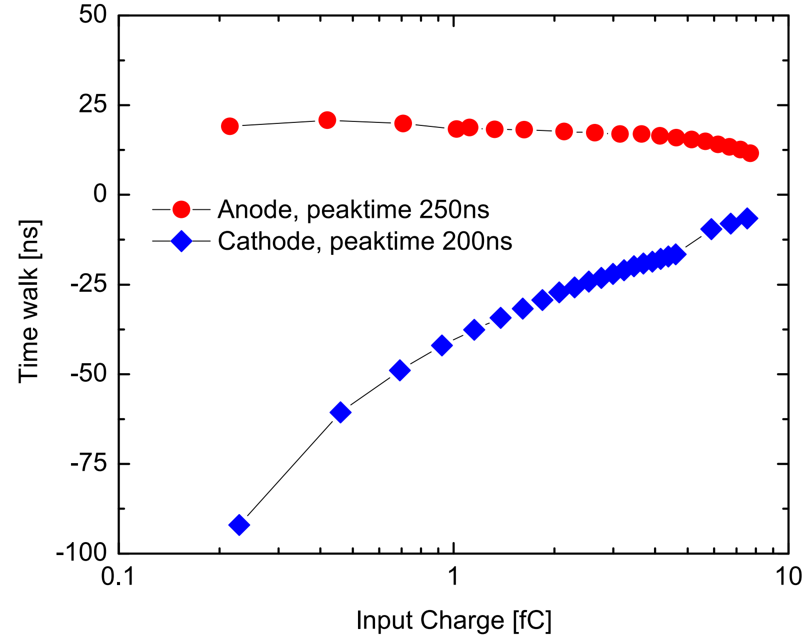
$$\sigma_t \approx \frac{ENC \cdot \tau_p \lambda_p}{Q\, \rho_p}$$

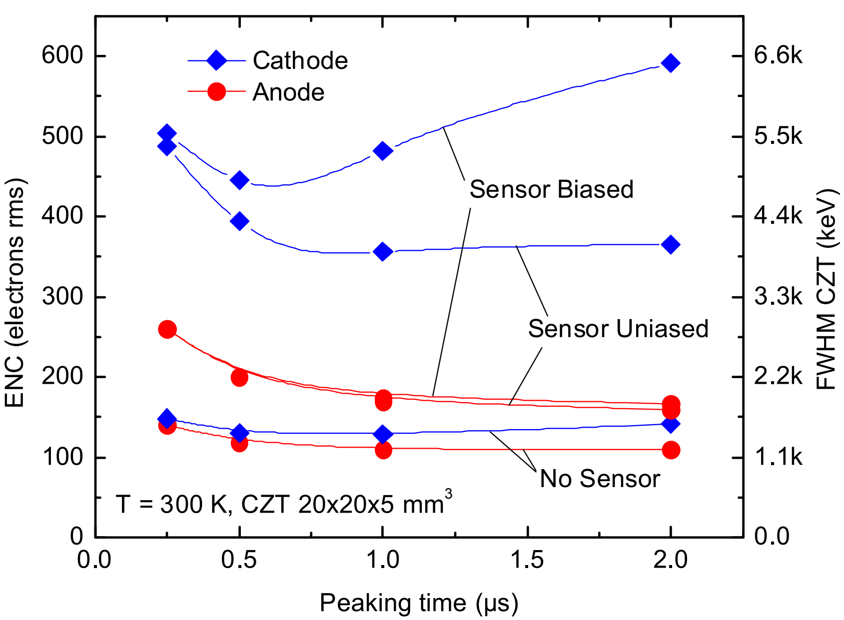
Shaper Coefficients for Amplitude and Timing Resolution

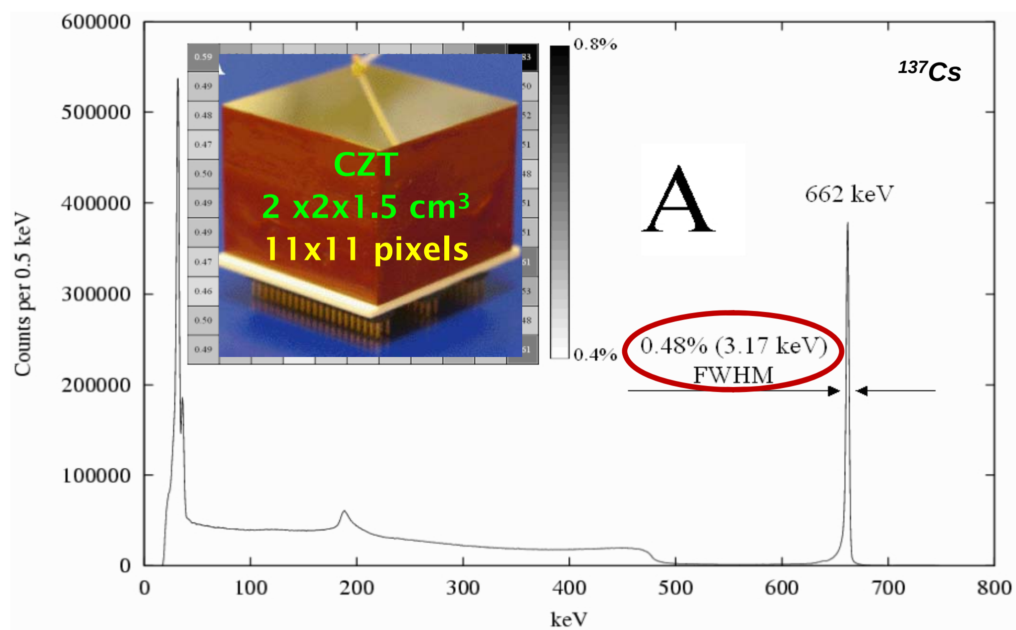
Filter	Shape	a_w	$a_f(1)$	a_p	$\rho_f(\alpha_f)=a_f(\alpha_f)/a_f(1)$	τ_w/τ_p	$-\rho_p$	η_p	λ_p
RU-2		0.92	0.59	0.92		7.49	0.98	-	-
RU-3		0.82	0.54	0.66		5.04	1.85	0.30	1.64
RU-4		0.85	0.53	0.57		4.17	2.50	0.44	1.60
RU-5		0.89	0.52	0.52		3.72	3.01	0.52	1.60
RU-6		0.92	0.52	0.48		3.46	3.40	0.57	1.61
RU-7		0.94	0.51	0.46		3.28	3.74	0.61	1.62
CU-2		0.93	0.59	0.88		6.17	1.05	-	-
CU-3		0.85	0.54	0.61		3.92	2.07	0.31	1.59
CU-4		0.91	0.53	0.51		3.16	2.95	0.48	1.57
CU-5		0.96	0.52	0.46		2.84	3.65	0.58	1.58
CU-6		1.01	0.52	0.42		2.66	4.22	0.63	1.60
CU-7		1.04	0.52	0.40		2.55	4.71	0.65	1.62
RB-2		1.03	0.75	1.01		16.6	0.34	0.29	-
RB-3		1.11	0.78	0.76		9.87	0.69	0.41	-
RB-4		1.30	0.81	0.66		7.67	0.98	0.47	-
RB-5		1.47	0.85	0.62		6.61	1.20	0.51	-
RB-6		1.61	0.87	0.59		5.96	1.39	0.54	-
RB-7		1.74	0.90	0.57		5.53	1.55	0.56	-
CB-2		1.08	0.80	1.02		12.9	0.47	0.33	-
CB-3		1.27	0.86	0.76		7.29	0.91	0.45	-
CB-4		1.58	0.93	0.67		5.58	1.32	0.52	-
CB-5		1.87	0.98	0.62		4.80	1.66	0.56	-
CB-6		2.10	1.03	0.60		4.39	1.92	0.58	-
CB-7		2.33	1.06	0.57		4.10	2.15	0.61	-

H3D Measurements

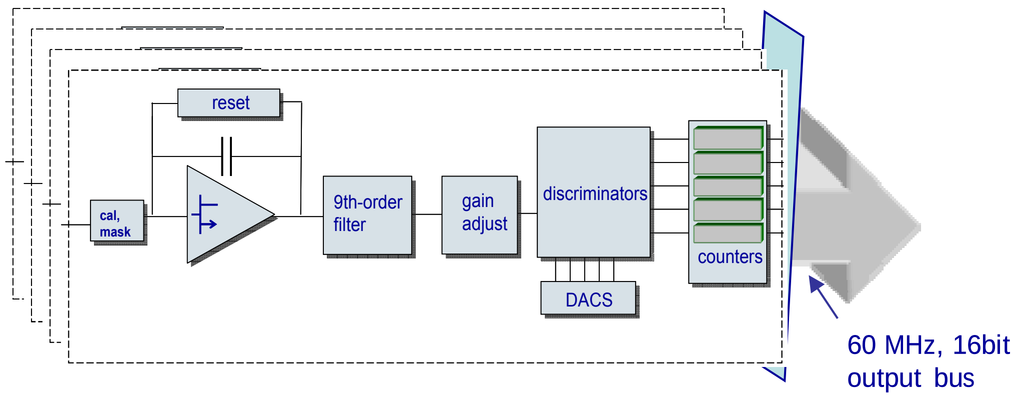


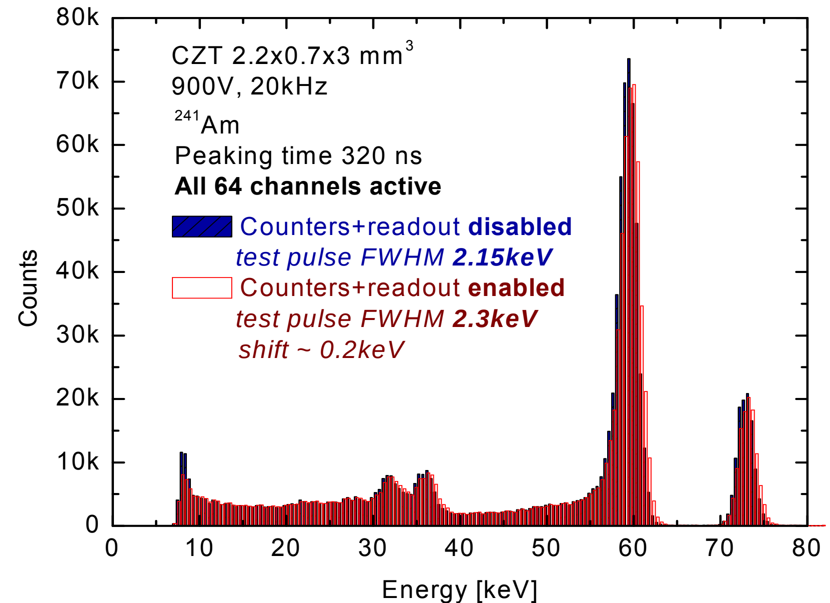


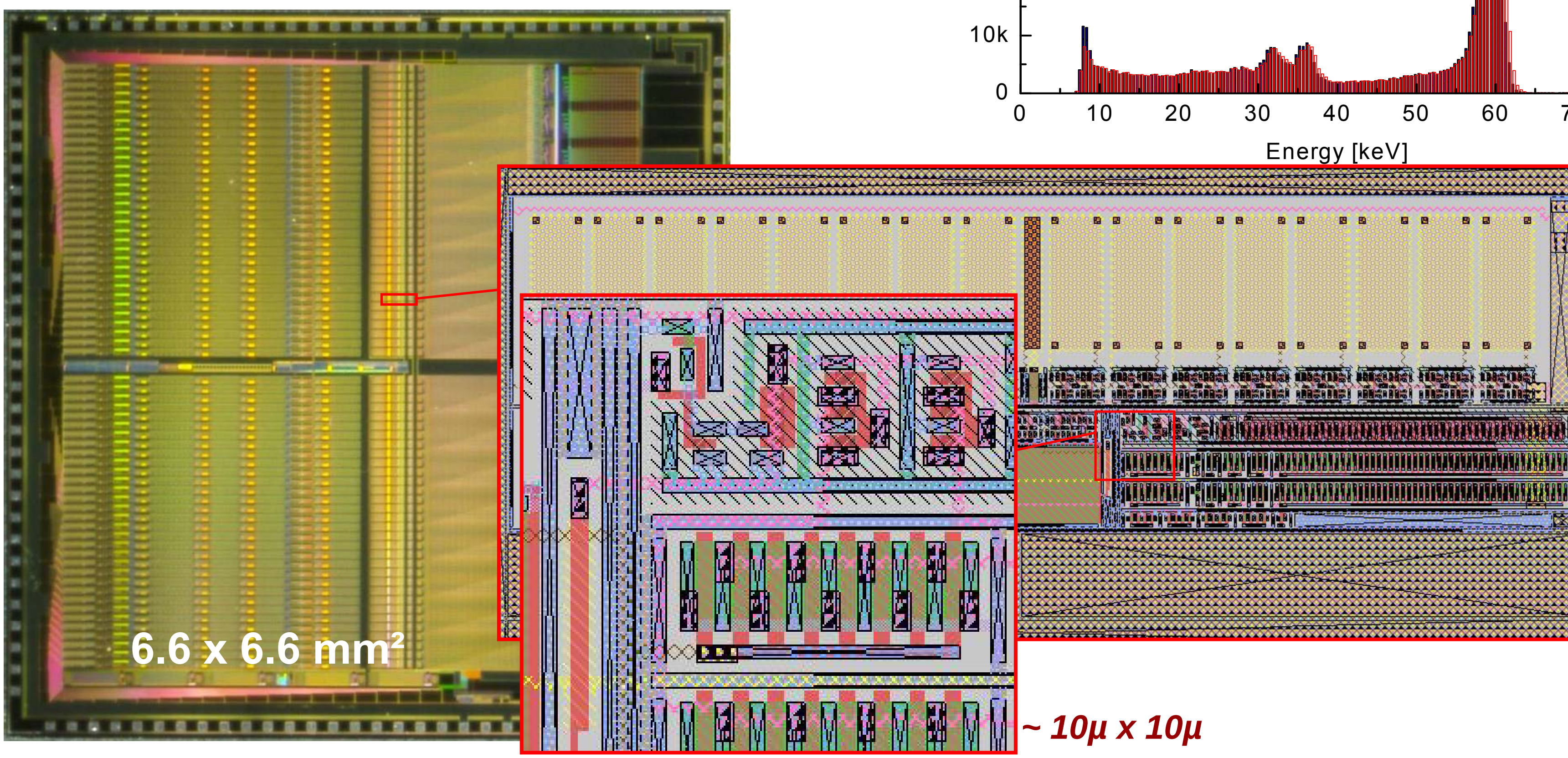




ASIC for High-rate Photon Counting Applications



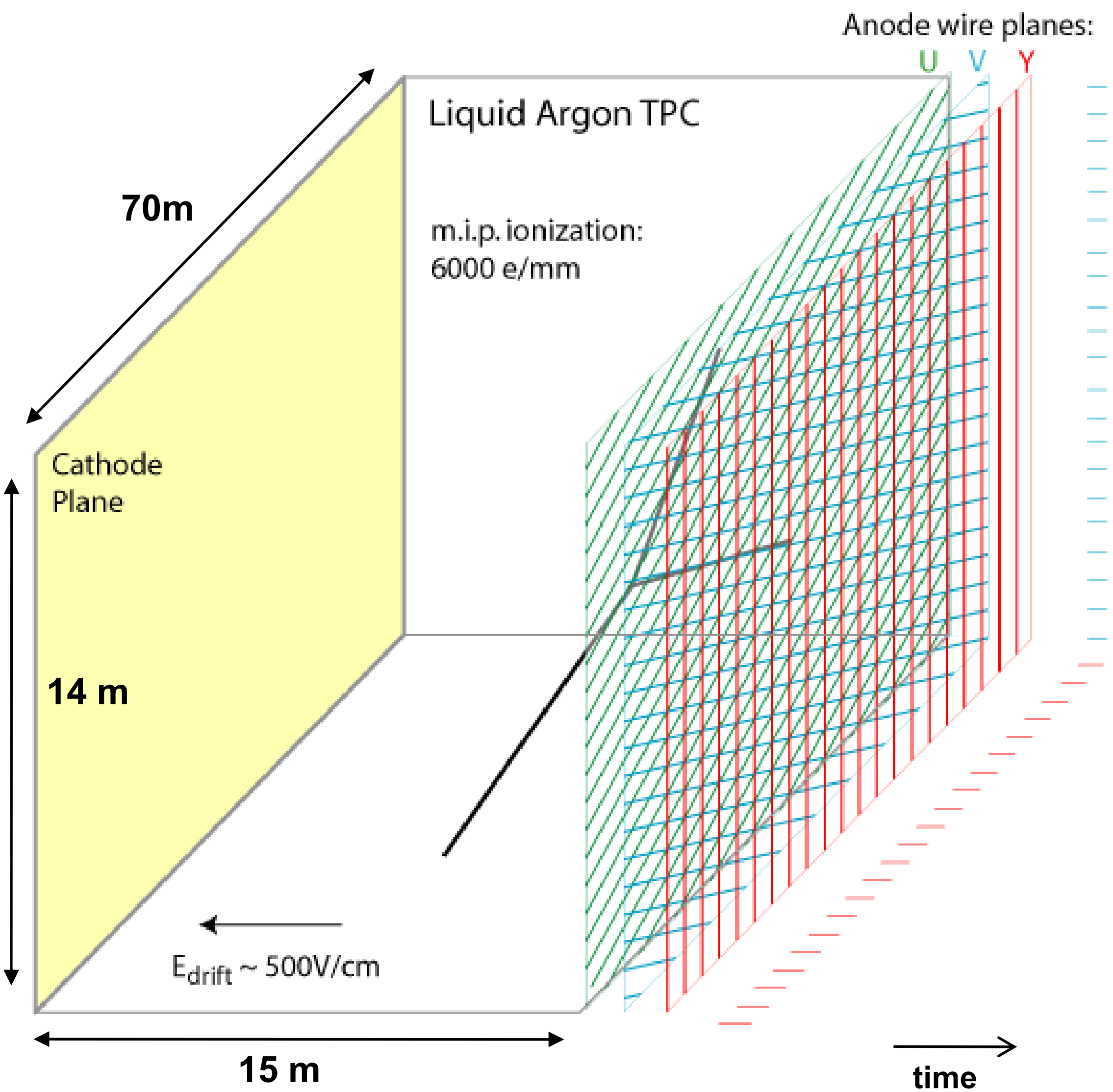




G. De Geronimo et al., IEEE TNS 54 (2007), collaboration with eV Microelectronics

LAr TPC Operation

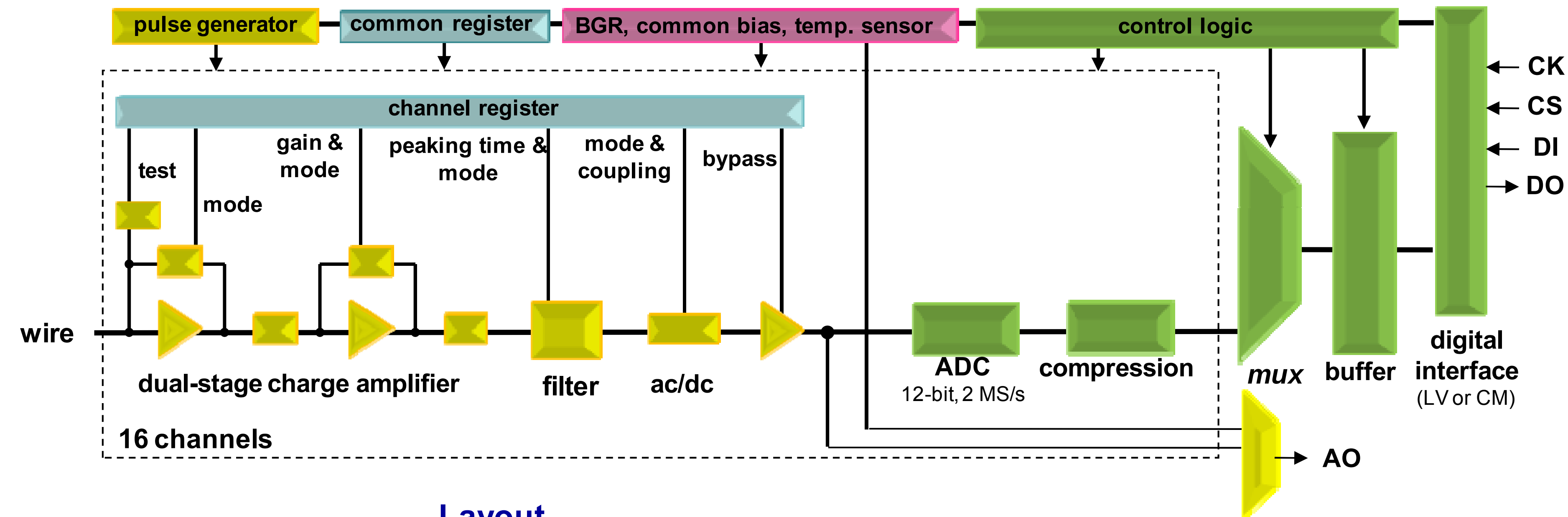
70 tons Liquid Argon Time Projection Chamber (LAr TPC), 800 feet underground in South Dakota at the Deep Underground Science & Engineering Lab (DUSEL) for Long Baseline Neutrino Experiments (LBNE)



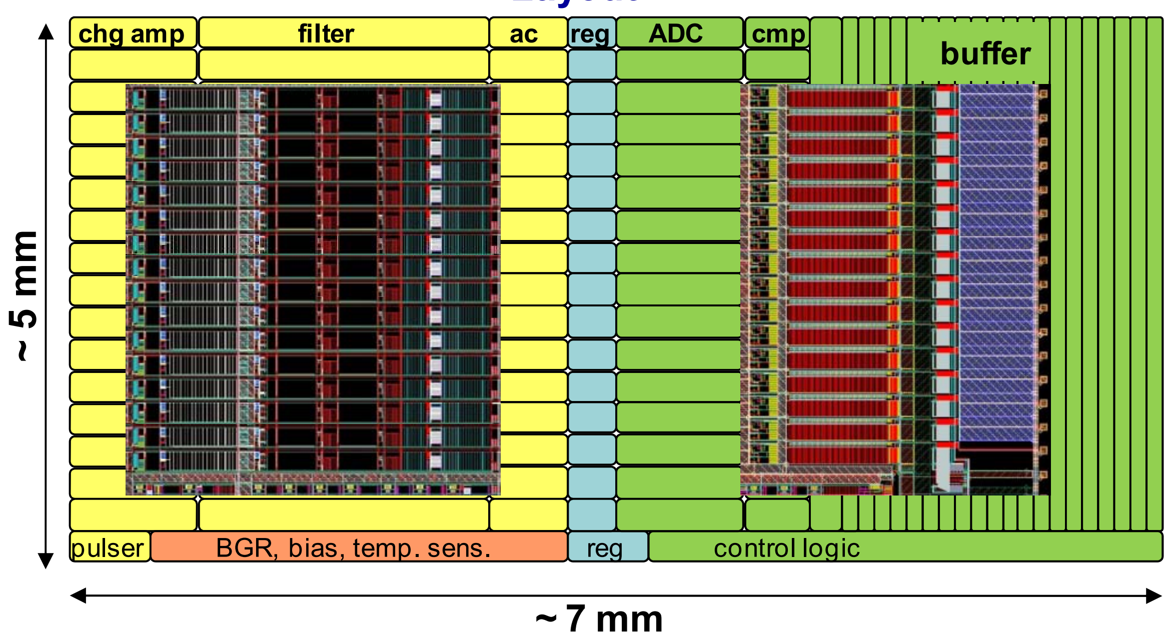
- **~ 600,000 anode wires**
  - **up to 200 pF**
  - **collecting (X)**
  - **non-collecting (U,V)**
- **charge amplification**
  - **range 300 fC**
  - **ENC < 1,000 e^-**
- **sample/buffer events**
  - **ADC 12-bit, 2 MS/s**
  - **3,000 deep buffer**
- **digital multiplexing**
  - **1000:1 multistage**
  - **collab. with FNAL**
- **power constraint**
  - **10 mW / channel**
- **operation in LAr**
  - **90K, > 15-20 years**

Mixed-Signal Front-end ASIC

Block Diagram



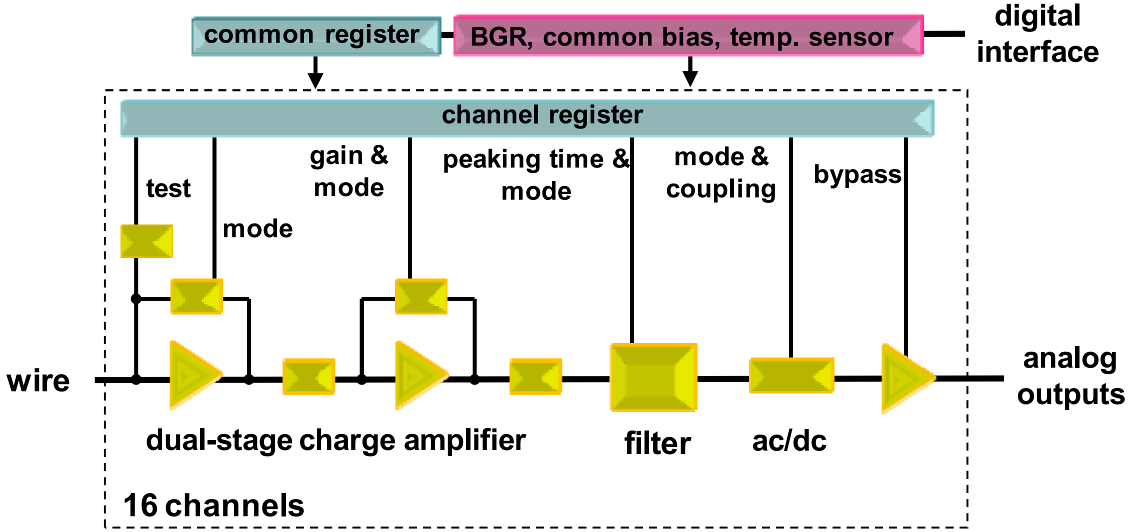
Layout

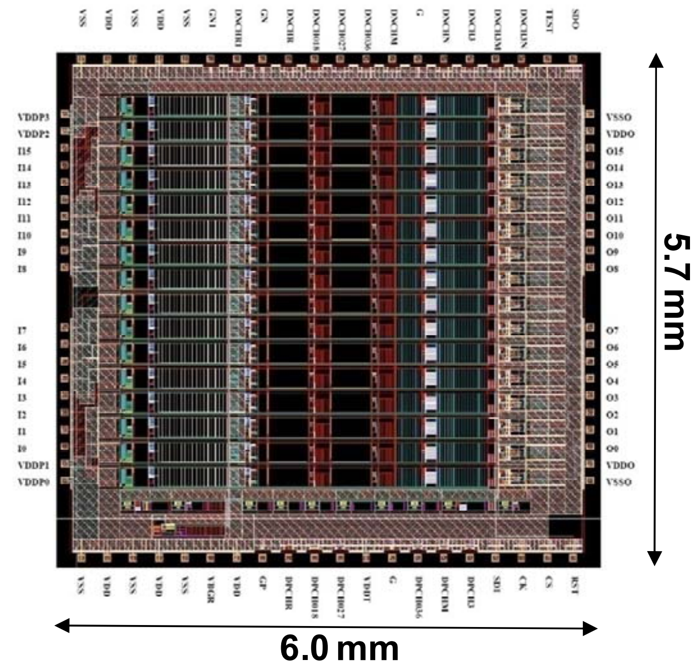


- 16 channels - mixed signal
- charge amplifier (adj. gain)
- high-order filter (adj. time constant)
- ac/dc, adjustable baseline
- test capacitor, channel mask
- ADC (12-bit, 2 MS/s)
- compression, discrimination
- multiplexing and digital buffering
- LV or CM digital interface
- pulse generator, analog monitor
- temperature sensor
- LAr environment (> 20 years at 90K)
- estimated size ~ 6 x 8 mm^2
- estimated power ~ 10 mW/ch.

Analog ASIC - Overview

Block Diagram



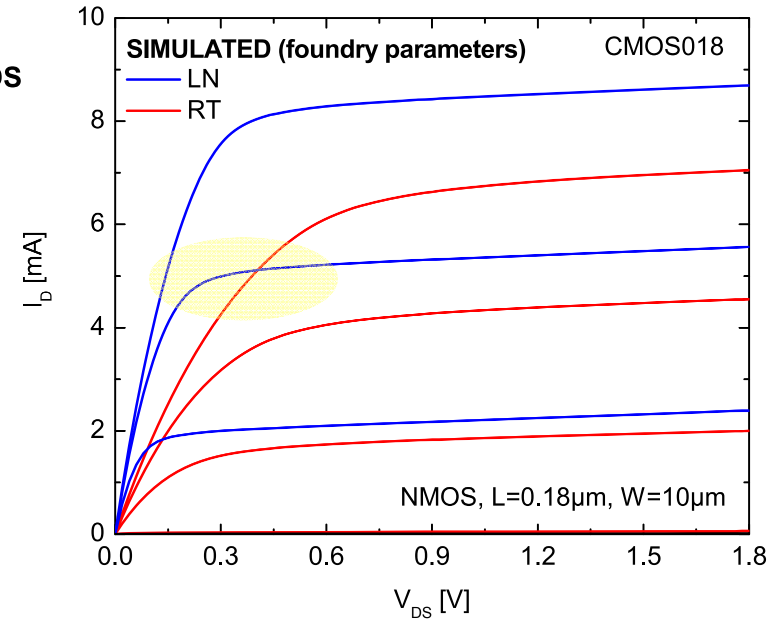


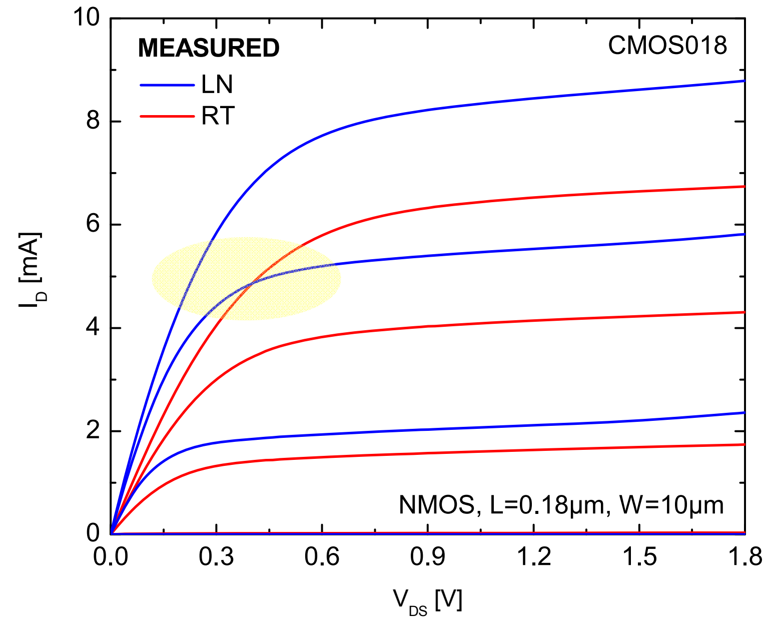
- 16 channels
- charge amplifier, high-order filter
- adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 μs)
- selectable collection/non-collection mode
  (baseline 200, 800 mV)
- selectable dc/ac coupling (100μs)

- rail-to-rail signal analog signal processing
- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- designed for room and cryogenic operation
- technology CMOS 0.18 μm, 1.8 V, 6M, MIM, SBRES

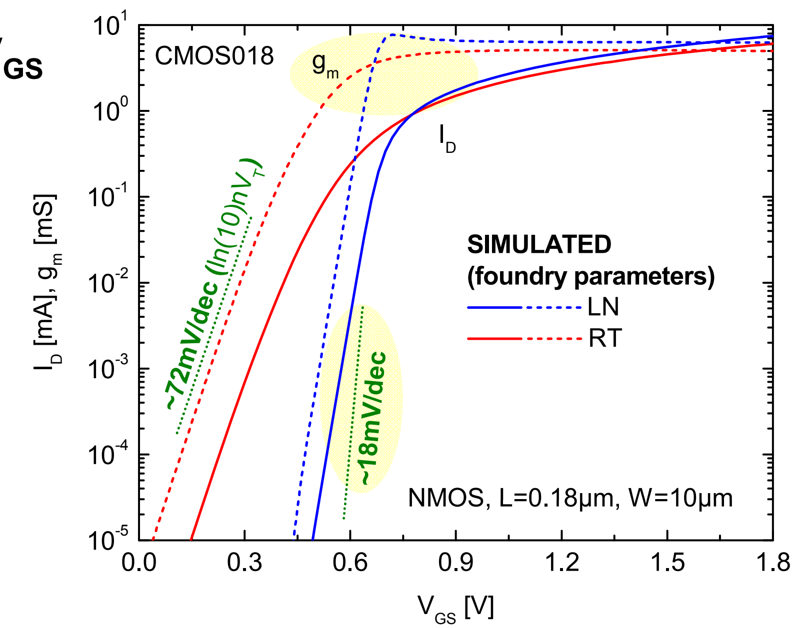
Static Model

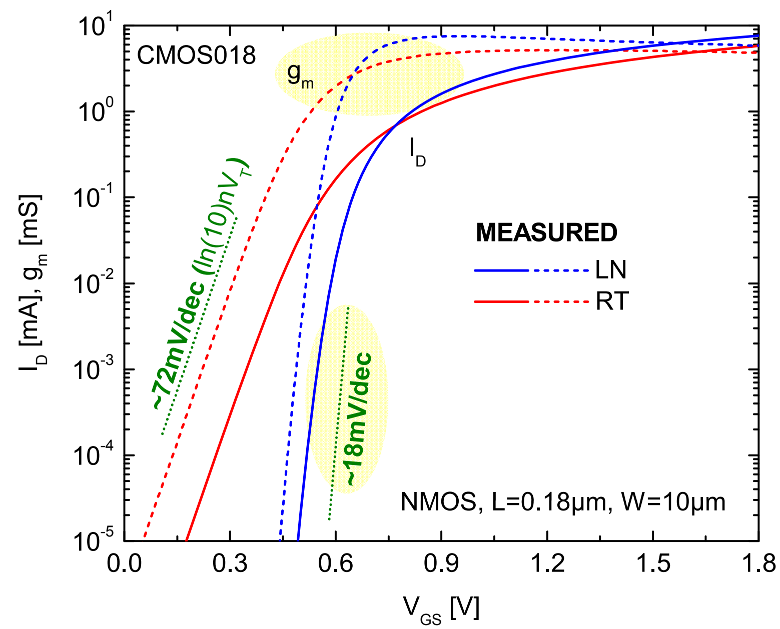
I_D vs V_{DS}





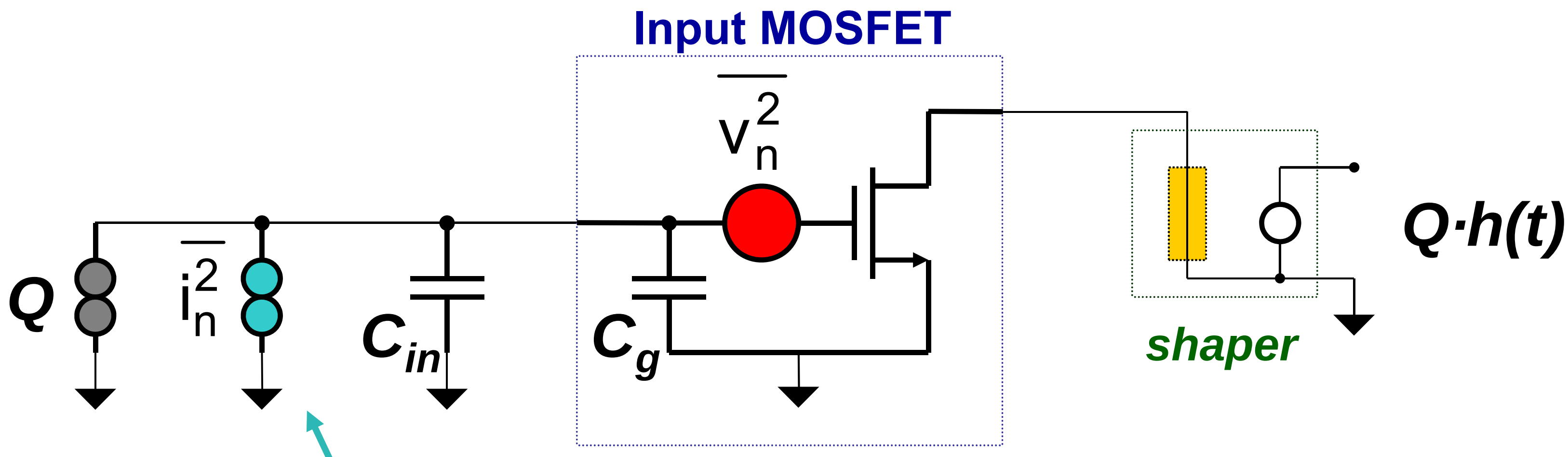
I_D vs V_{GS}





Some differences in saturation voltage, sub-threshold slope, transconductance

Input MOSFET Optimization



low-frequency (1/*f*)

white (thermal)

$$ENC^2 = a_p S_p \tau_p + \left(C_{in} + C_g\right)^2 \left(a_f A_f 2\pi + a_w \frac{S_w}{\tau_p} \right)$$

Noise Model: White

low-frequency ***white***

$$S_v \approx \frac{K_f(IC,L,T)}{C_{ox}WLf^{\alpha_f(IC,L,T)}} + \alpha_w(IC,L,T)\,n\,4kT\,\frac{\gamma(IC)}{g_m(IC,L,T)}$$

$n \approx 1.3$

$\mu_{77K} \approx 5\times\mu_{300K}$

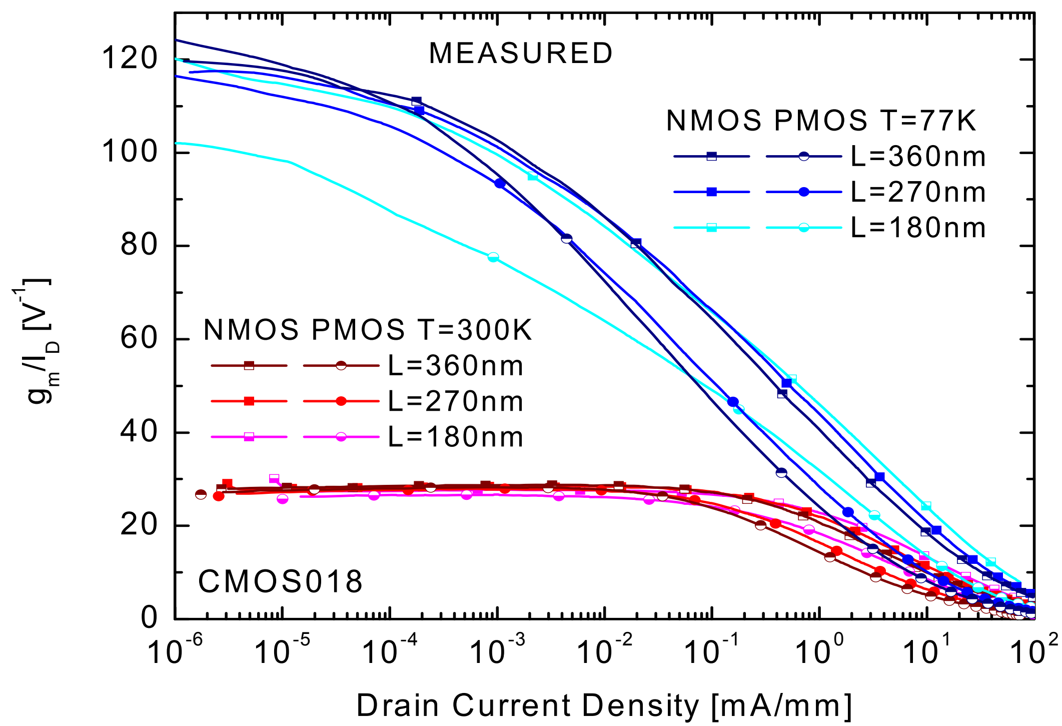
$IC_{77k} \approx 3\times\mu_{300K}$

$$\gamma \approx \frac{1}{1+IC}\left(\frac{1}{2}+\frac{3}{2}IC\right)$$

$$IC = \frac{I_D}{2n\mu(T)C_{ox}\frac{W}{L}V_T^2}$$

Inversion Coefficient

g_m/I_D

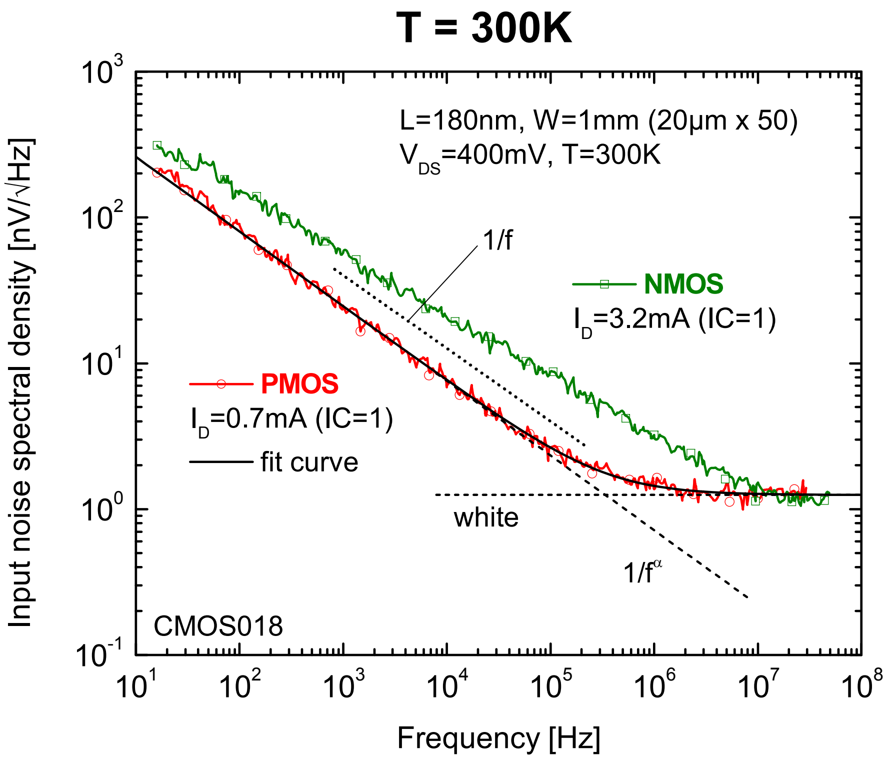


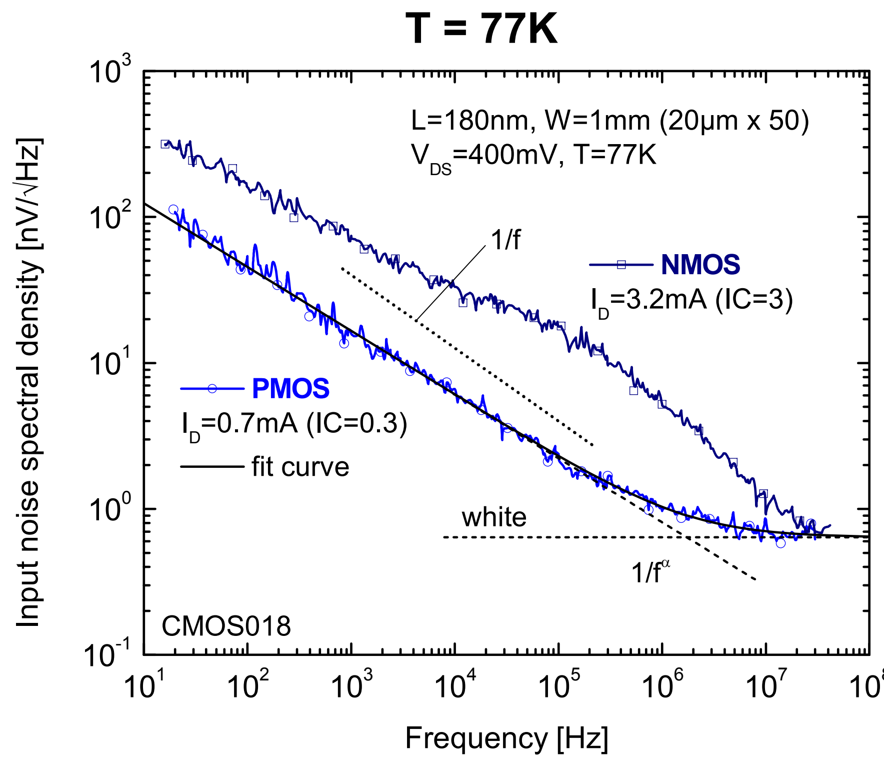
At given current, white noise decreases since

- **T decreases**
- **g_m increases**

$$\frac{g_m}{I_D} \to \frac{q}{nk_BT} = \begin{cases} \sim 30 \text{ at } T = 300K \\ \sim 116 \text{ at } T = 77K \end{cases}$$

Noise Model: Low-Frequency



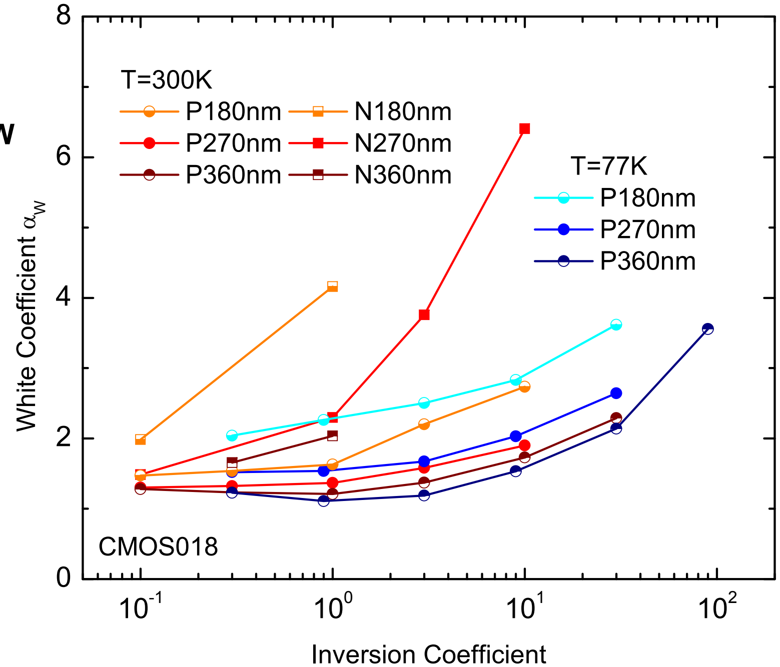


- comparable K_f
- different slope
  - > 1 in PMOS
  - < 1 in NMOS

- lower white noise
- NMOS
  - comparable K_f
  - lorentzian packet
- PMOS
  - lower K_f
  - lower slope < 1

Summary of Noise Coefficients

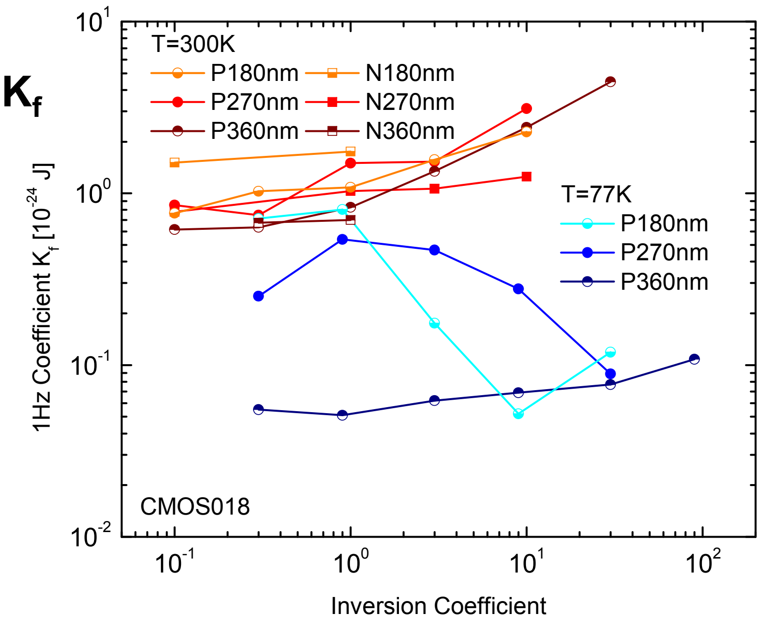
white excess coefficient α_W



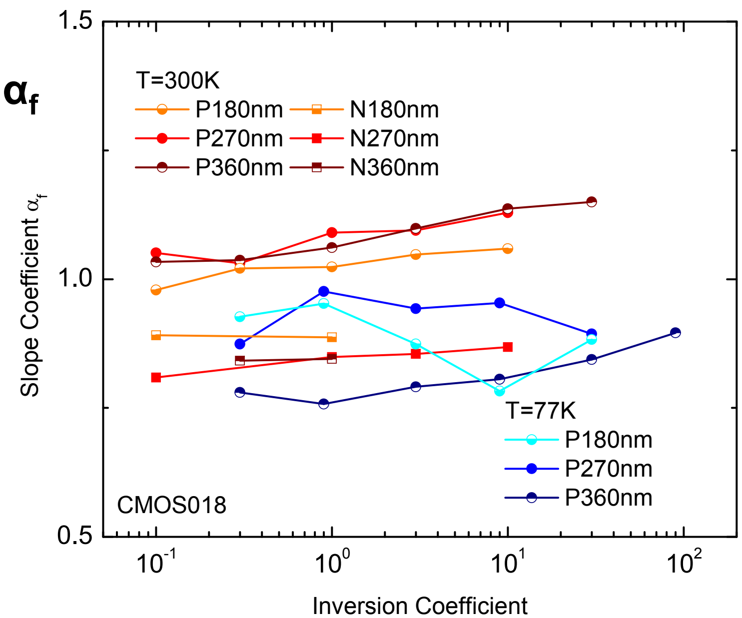
- **always larger than unity**
- **general increase with**
  - **drain current density**
  - **inverse of channel length**
  - **inverse of temperature**

- **somewhat dependent on fitting**
- **increase in K_f associated with increase in slope**

K_f

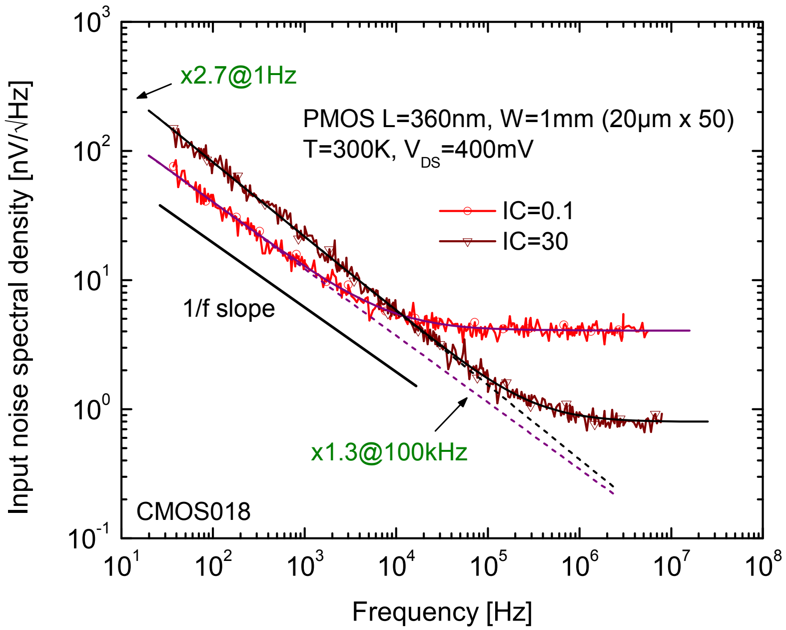


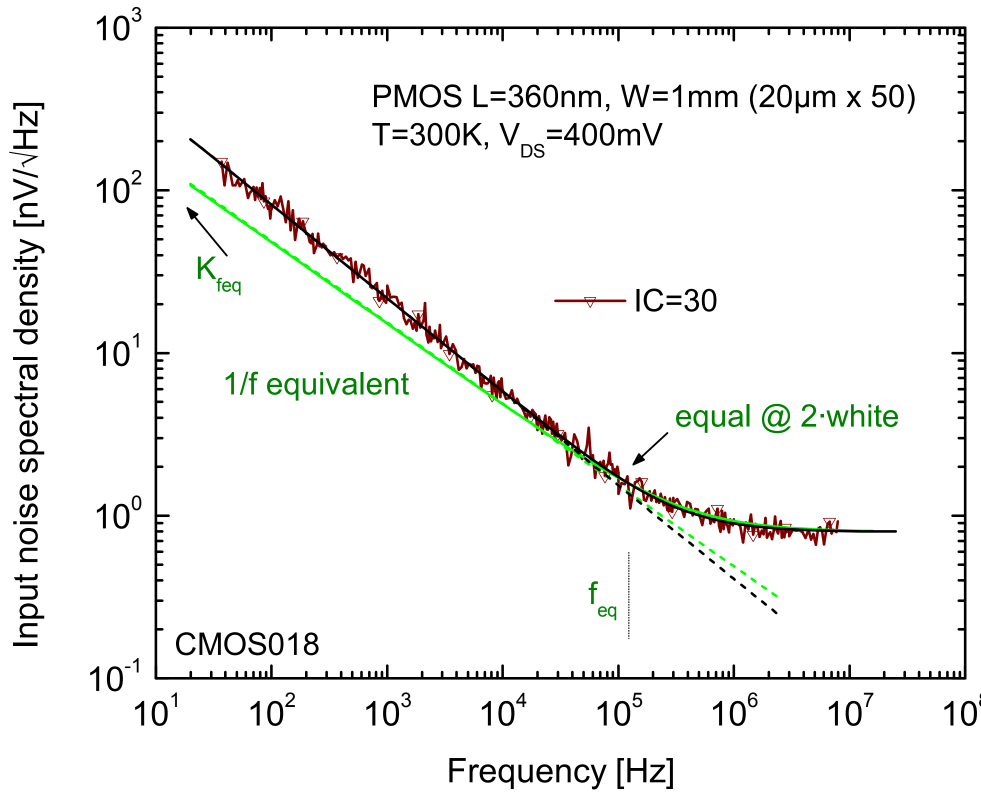
α_f



Equivalent 1/f (K_{feq})

PMOS 360nm at 300K,
35 µA/mm and 11 mA/mm





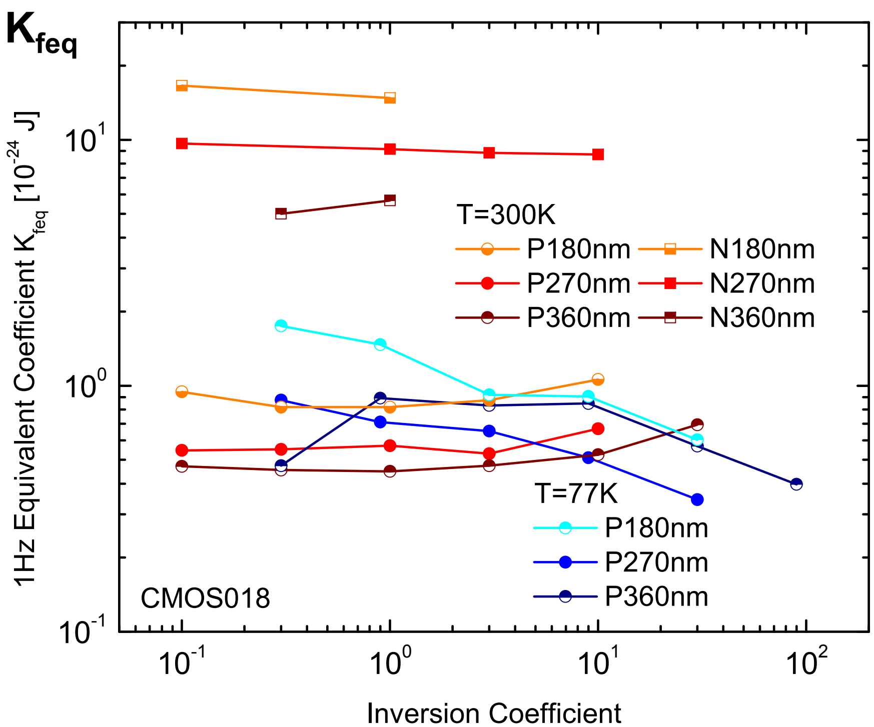
- **as K_f increases, slope increases (α_f increases)**

Equivalent 1/f: equal value at twice the white component (four times in power)

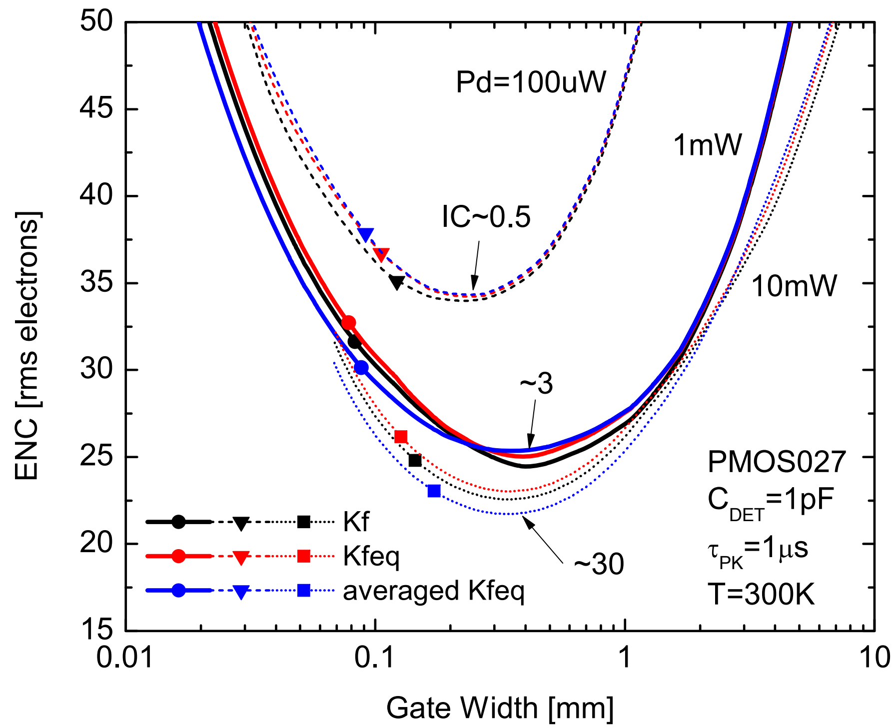
$$\frac{K_{feq}}{C_{ox}WLf_{eq}} + \text{white} = S_v\left(f_{eq}\right) \quad \text{where} \quad S_v\left(f_{eq}\right) = 4 \times \text{white}$$

$$\Rightarrow K_{feq} = C_{ox}WLf_{eq}3 \times \text{white}$$

Equivalent 1/f (K_{feq})



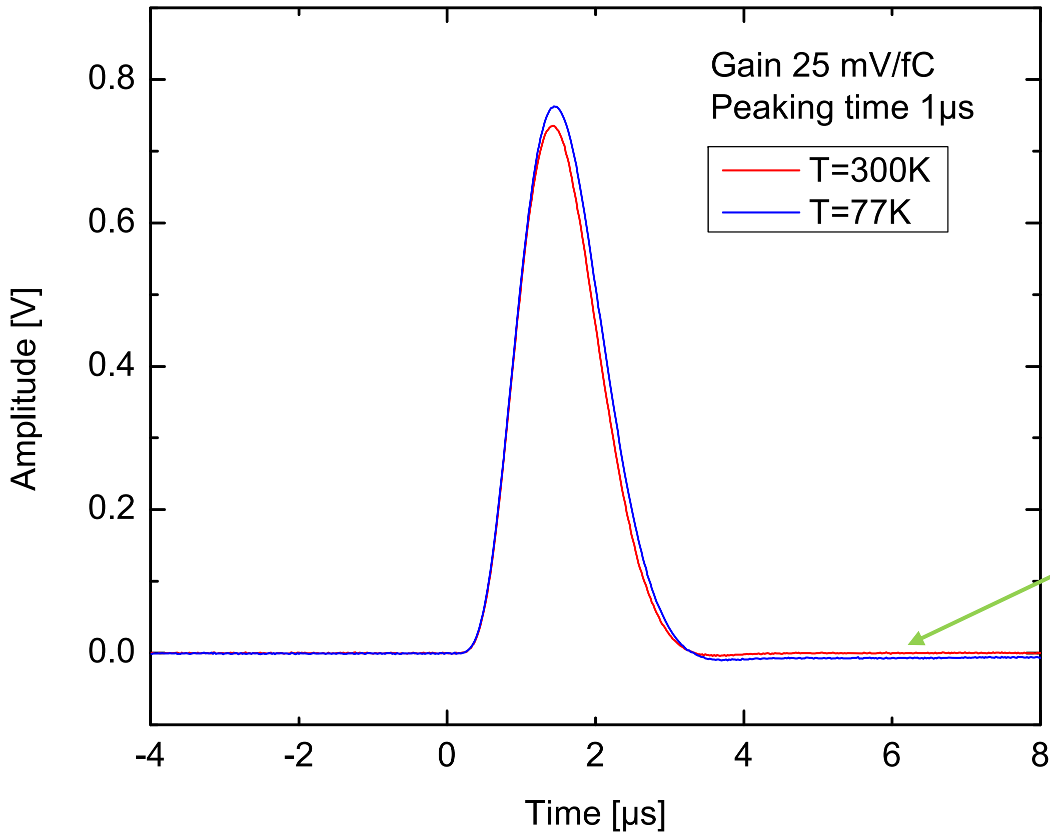
Optimum W: example for 1pF



• **dependence of K_{feq} on drain current density is now modest**

• **negligible error in optimization**
• **some error in estimate for large relative power (large mW/pF)**
• **averaged K_{feq} can also be used**

Analog ASIC - Signal Measurements



Bandgap Reference

$$V_{BGR} \approx \begin{cases} 1.185\ \text{V} & \text{at } 300\ ^\circ\text{K} \\ 1.164\ \text{V} & \text{at } 77\ ^\circ\text{K} \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor

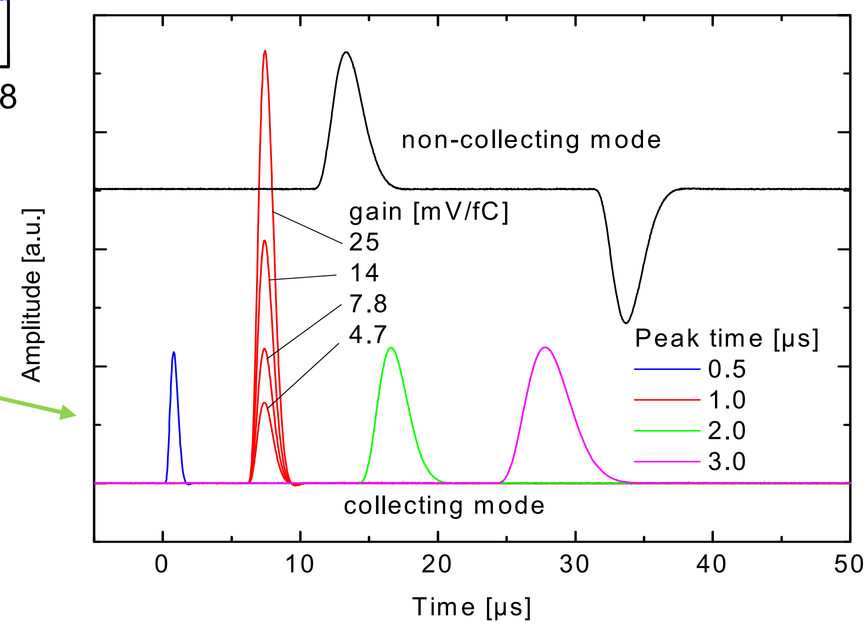
$$V_{TMP} \approx \begin{cases} 867.0\ \text{mV} & \text{at } 300\ ^\circ\text{K} \\ 259.3\ \text{mV} & \text{at } 77\ ^\circ\text{K} \end{cases}$$

~ 2.86 mV / °K

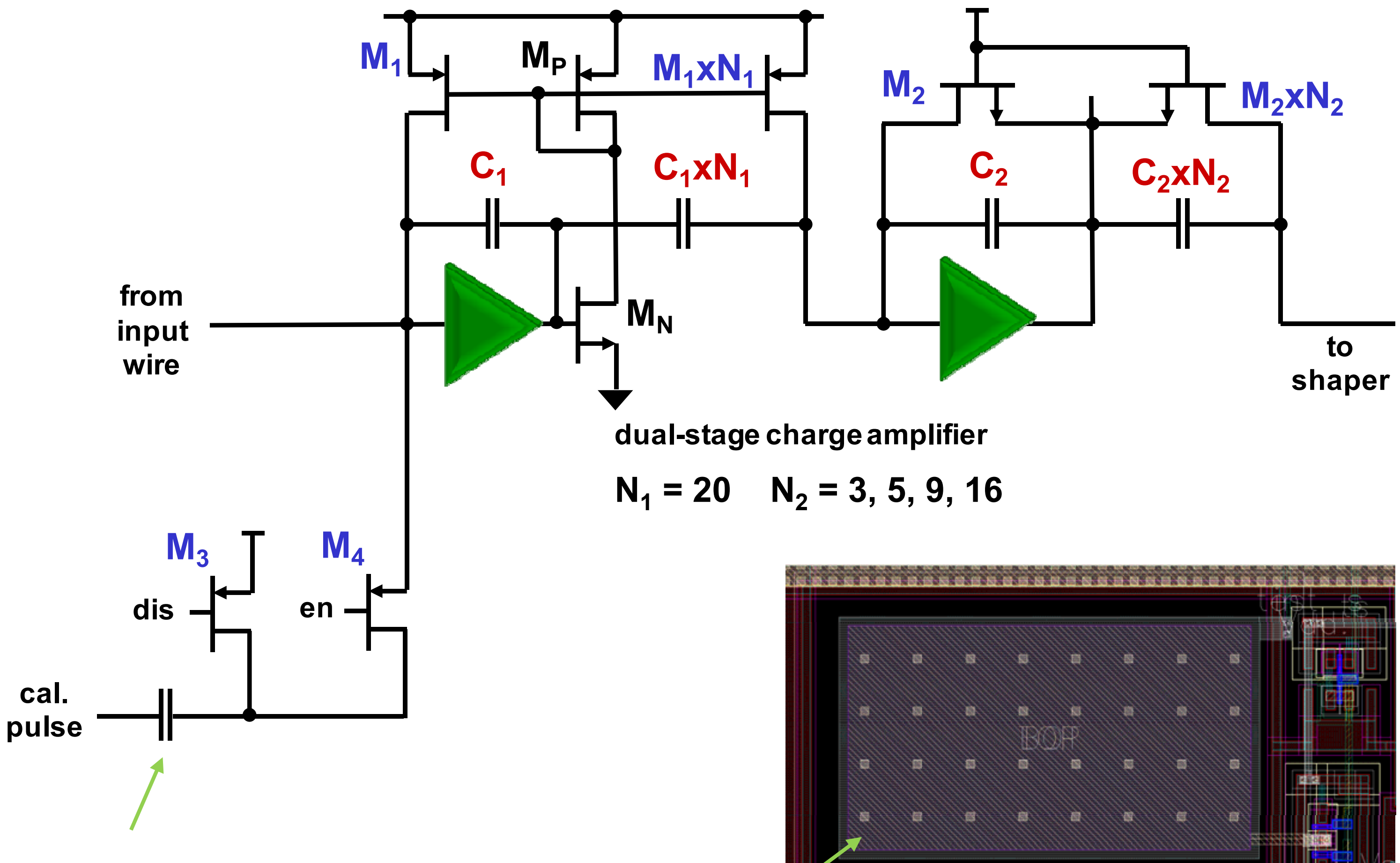
Pole-zero cancellation at 77K to be addressed in next revision

Adjustable gain, peaking time and baseline

maximum charge 55, 100, 180, 300 fC



Analog ASIC - Front-end Detail and Calibration Scheme



$C_{INJ} \approx 180$ fF

Integrated injection capacitance (10 x 18 µm²)

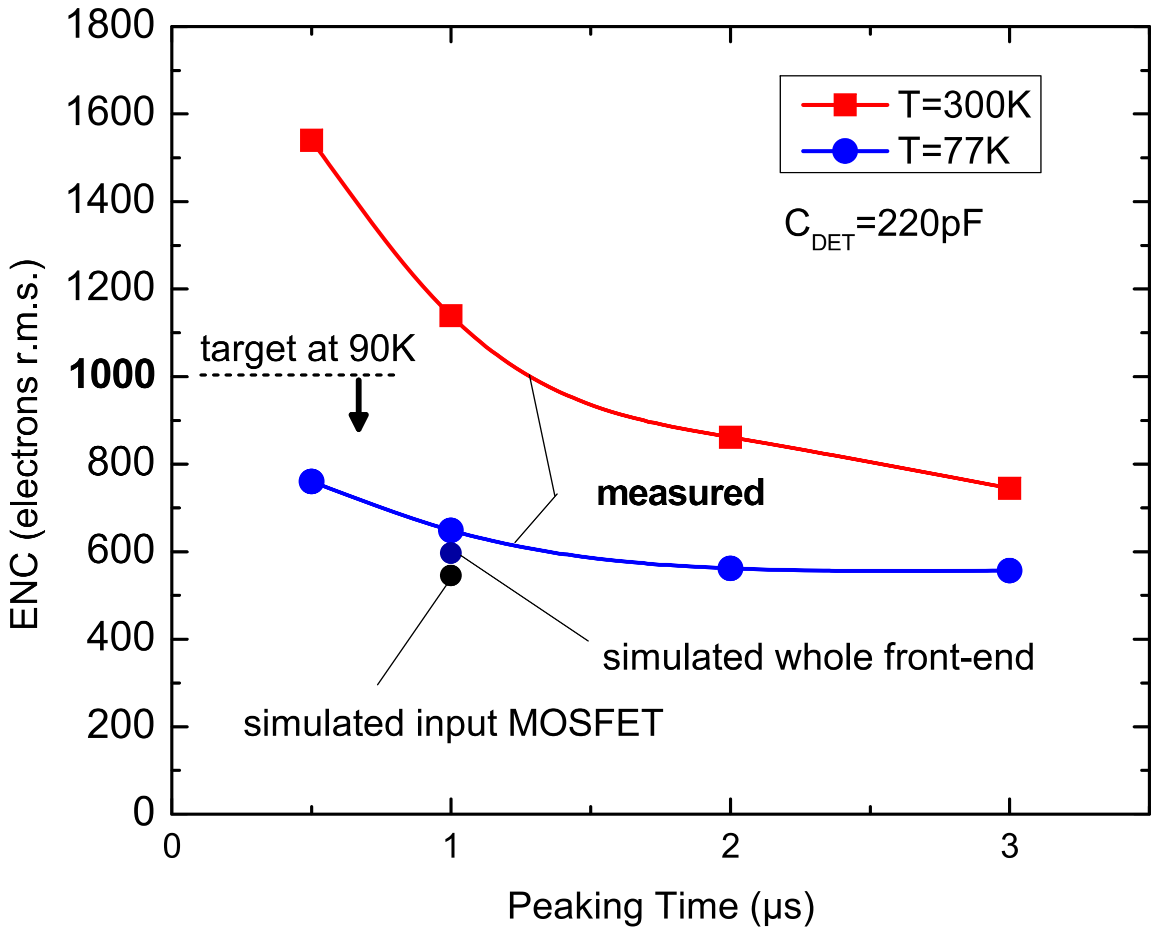
Disabled (grounded) when unused

Measured with high-precision external capacitor

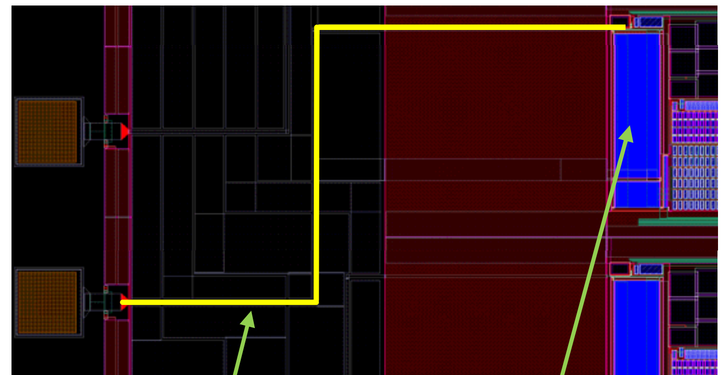
$$C_{INJ} \approx \begin{cases} 184\ \text{fF} \quad \text{at}\ \ 300\text{K} \\ 183\ \text{fF} \quad \text{at}\ \ 77\text{K} \end{cases}$$

$$\text{variation} \approx 0.5\%$$

Analog ASIC - Noise Measurements

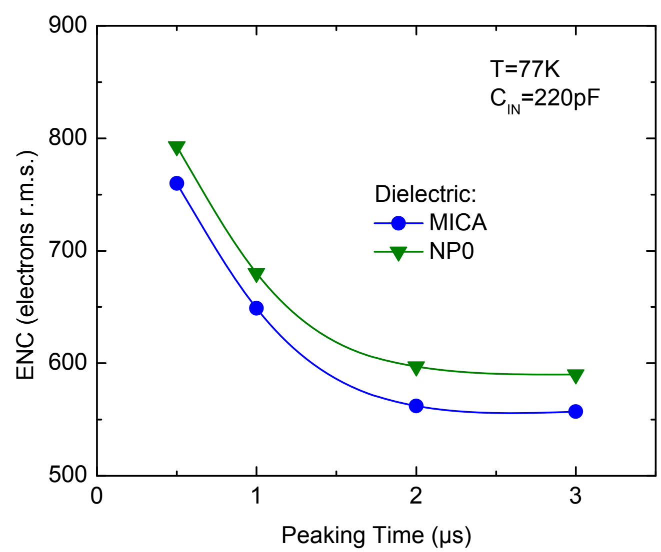


Layout Detail



Input Line
L ≈ 1 mm
W = 3.5 μm
(M3 + M4)
R_{77K} ≈ 3 Ω
R_{300K} ≈ 12 Ω

Input MOSFET
L = 270 nm
W = 10 mm
(50μm x 200)
$g_{m,77K}$ ≈ 90 mS (11 Ω)
$g_{m,300K}$ ≈ 45 mS (22 Ω)



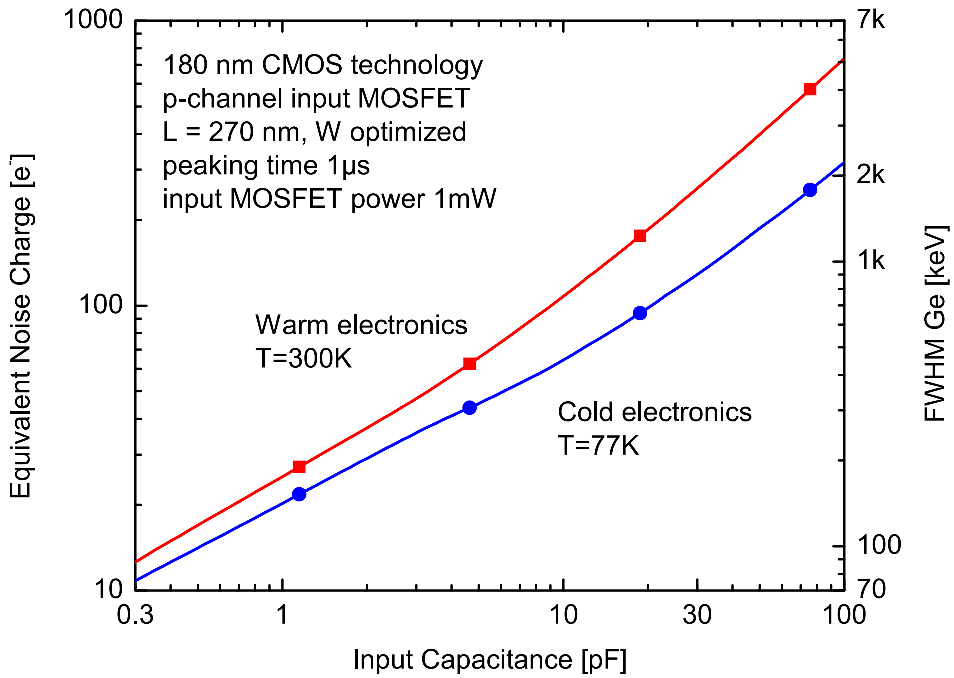
Measurements include:

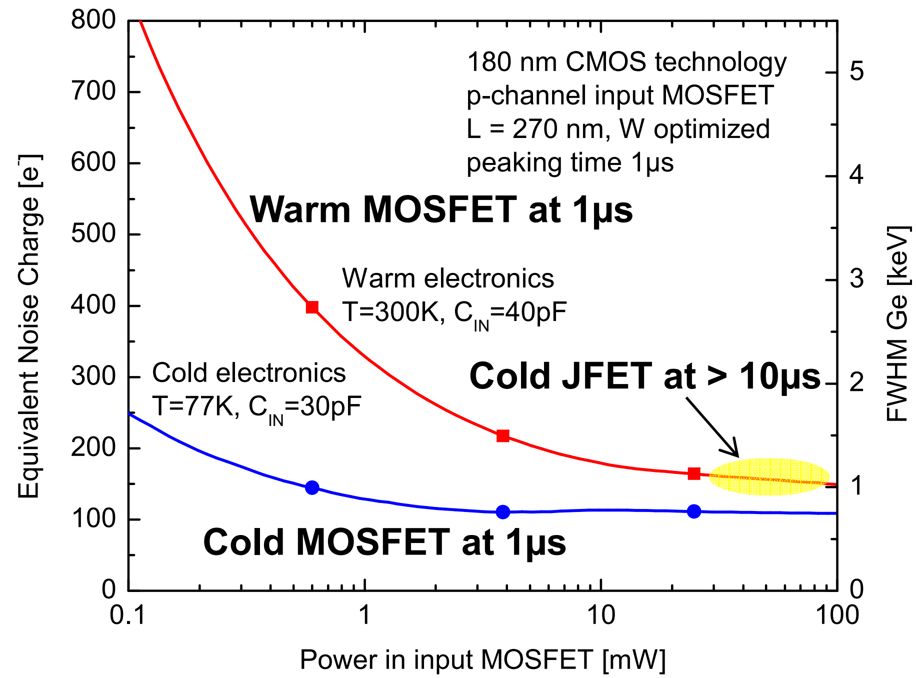
- **input line parasitic resistance**
  - **~ 150 e^- at 77 K (~ 590 e^- at 300K)**
  - **addressed in next revision**
- **C_{IN} dielectric noise (not present in wire)**
  - **~ 60 e^- at 77 K**

$$dENC \approx \sqrt{2kTC_{IN}tg\delta}$$

$$\approx \begin{cases} 200\,e^- \text{ for NPO} \\ 60\,e^- \text{ for MICA} \end{cases}$$

Prospects for Germanium Sensors





- **Compared with cold JFET**:
  - **warm MOSFET offers similar resolution at shorter peaktime**
  - **cold MOFET offers higher resolution at lower power and shorter peaktime**
    - higher functionality increases signal integrity
    - multiplexing reduces cryostat feed-throughs
    - shorter peak-time allows higher rate and reduces microphonics

- Actual energy resolution about **10-20% higher** (contribution from the next stages)
- Power in **input MOSFET includes input branch**
- Power **dissipated by the next stages** must be included (from few tens of µW to few mW depending on the required linear dynamic range)

Conclusions and Future Work

- **ASIC design process is defined and predictable**
- **ASICs offer**
  - **high resolution and high functionality at low power**
  - **high yield, high reliability, long lifetime**
- **Mixed-signal circuits are compatible with low-noise front-ends**
- **ASICs are "happier" in cryogenic environment, offering a valuable solution for a number of detectors/applications**

Acknowledgment

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University of Michigan

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