Tipp 2011

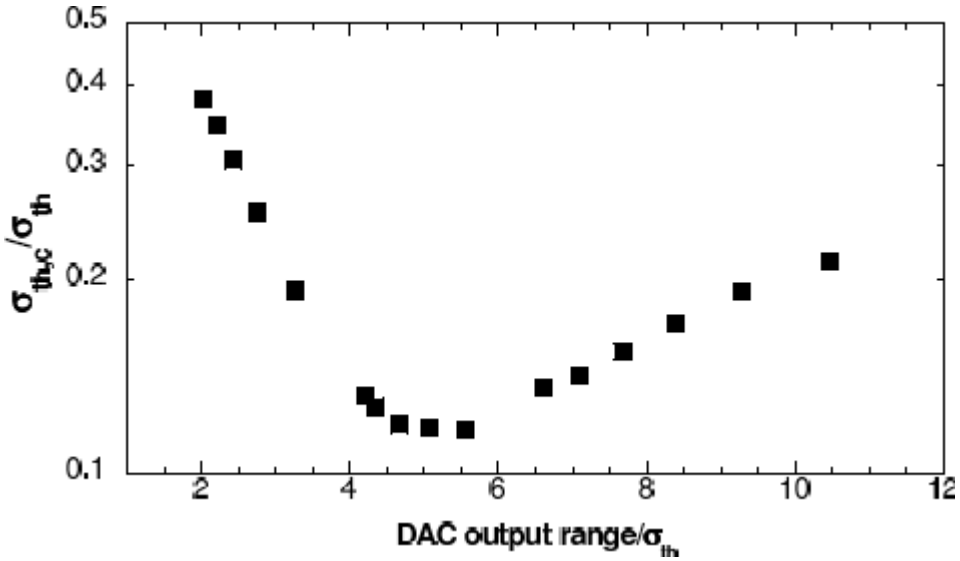
FEE TRACK SUMMARY

JP WALDER

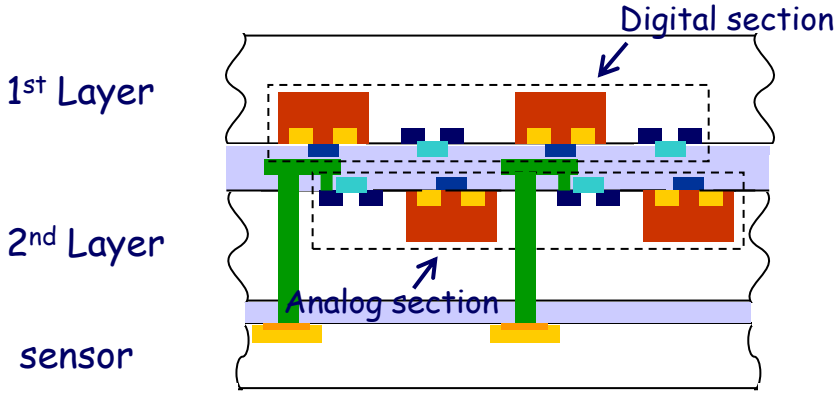
- ✓ Most of CMOS and SOI designs are using 0.35um → 0.12um
  We are the first designing a mixed mode circuit in 65nm..
- ✓ Presentation from Bob, Carl, Devis and Lea went well and triggered questions and comments.
- ✓ Valerio Re (INFN): 3D pixel chip using Tezarron for SuperB.

Superpix1: a 3D CMOS chip for 50x50 um^2 pixels

- This plot shows that an optimum condition exists for the threshold correction operation (DAC output range ≈5σ_{th}):



To be connected to a high resistivity pixel sensor



Charge sensitivity	48 mV/fC
Peaking time @ 16000 injected electrons	260 ns
ENC	130 e-
Threshold dispersion before/after correction	560/65 e-
Analog power consumption	10 µW/pixel
Detector capacitance	150 fF
Matrix size	128x32 pixels
Pixel pitch	50 µm

The readout architecture is the same as in the 3D MAPS device

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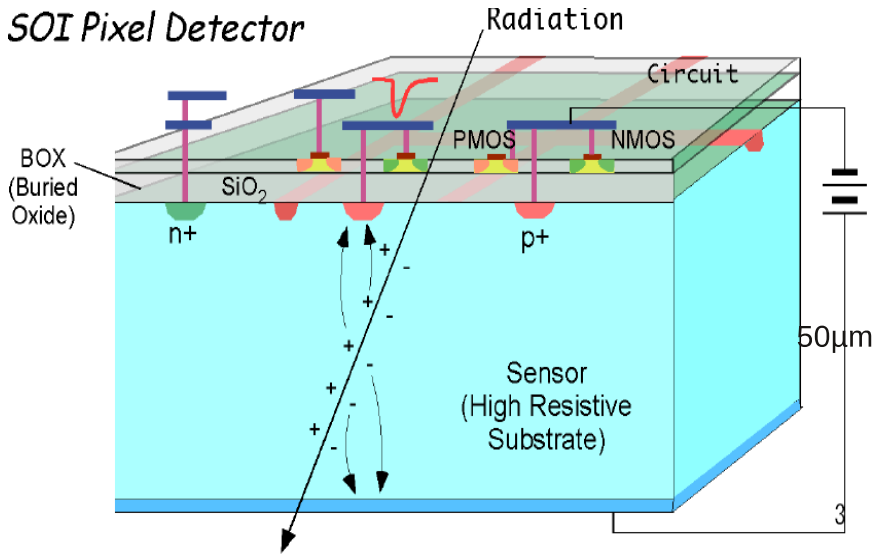
Process: Silicon on Insulator

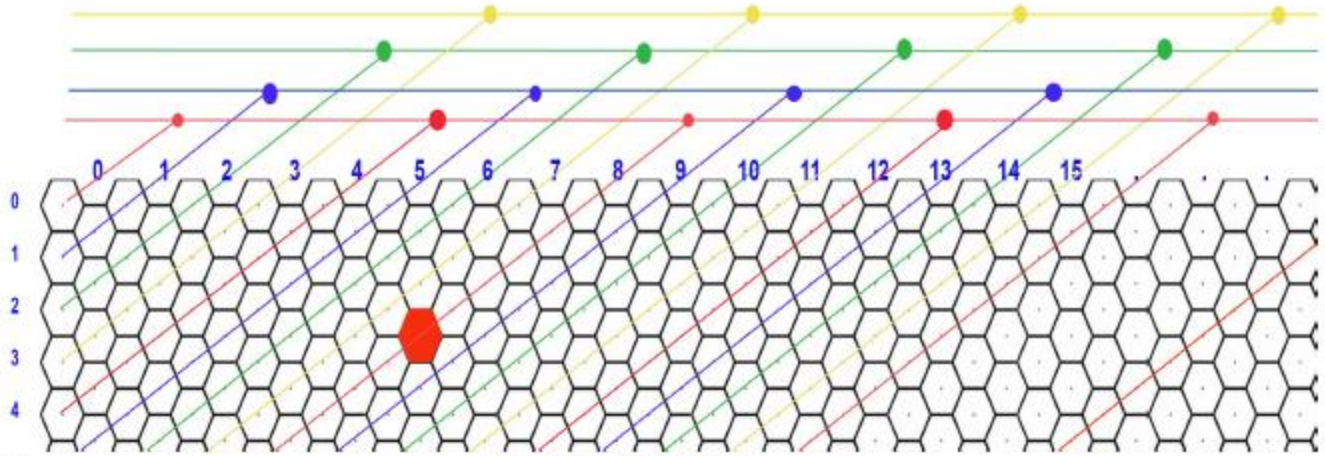
- ROHM Semiconductor
  - 0.2µm
- Designs include:
  - CAP5, CAP7, CAP9, CAP11, CAP12
  - Process actively researched
  - Designed for detectors by ROHM/OKI Semiconductor
  - Continued development with collaborators:
    - KEK, ROHM/OKI, FNAL, LBNL, UH



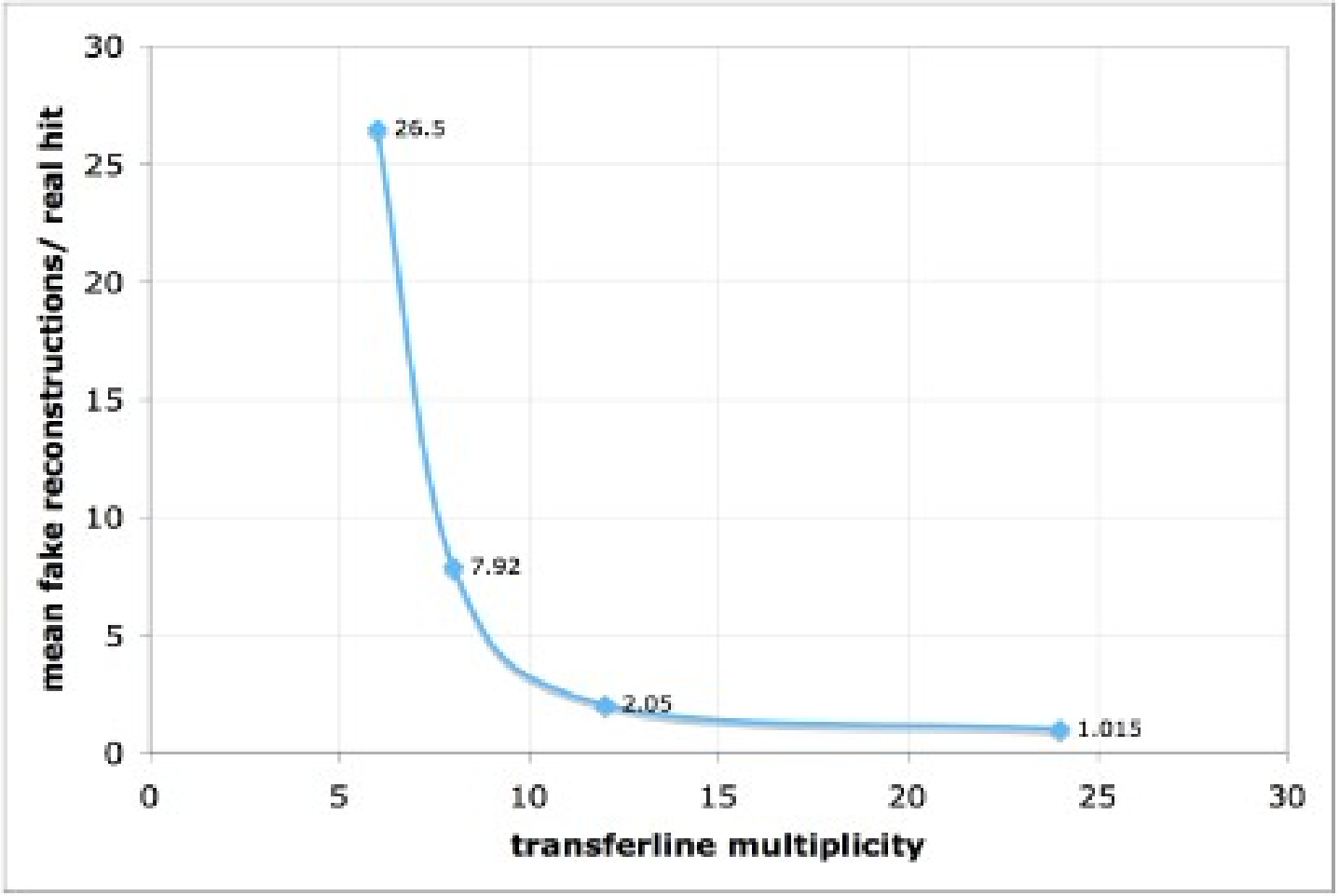
Charge collection mechanism in SOI process.

Readout Type: Hexagonal

- Each pixel outputs binary signal in three directions to periphery (CAP9)
- Multiple rows of shifting logic (TLM)
  - More transfer lines = higher readout speed



TLM Effectiveness



detector	matrix	pitch	shift clock	outputs	(effective) occupancy
binary	800x240	25 µm square	2 MHz (internal lines)	480	0.124
binary	800x240	25 µm square	10 MHz (internal lines)	480	0.005
binary hexagonal TM = 8	960x240	25 µm hexagonal	100 MHz (external lines)	48	2.2E-04
binary hexagonal TM = 12	960x240	25 µm hexagonal	100 MHz (external lines)	72	5.2E-05
binary hexagonal TM =24	960x240	25 µm hexagonal	100 MHz (external lines)	144	2.7E-05
analog rolling shutter	420x120	50 µm square	9 µs integration time	120	0.016

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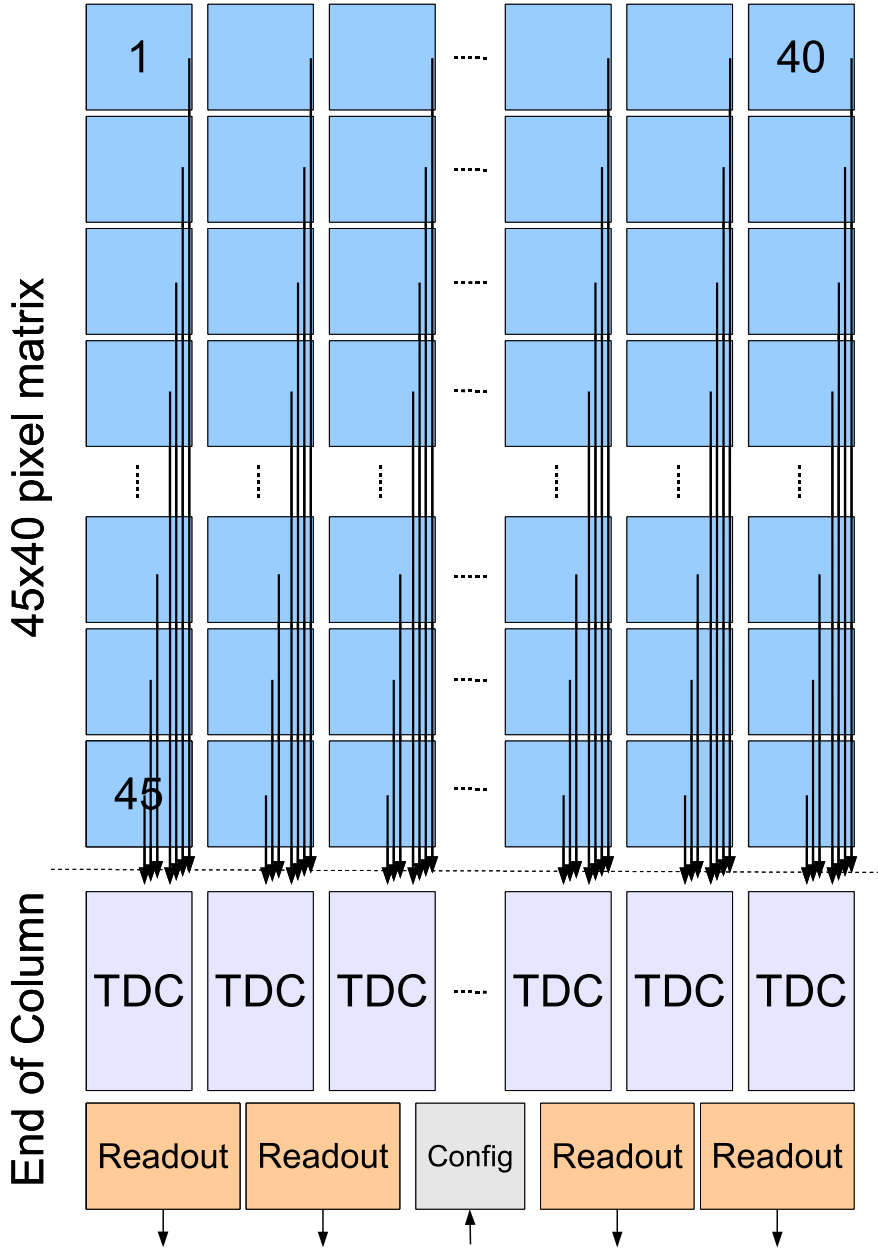
TDCpix block diagram

Requirements

- 45 x 40 pixel channels
  300 x 300 μm²
- Chip hit rate ~130 MHz
- Timing resolution 200 ps RMS
- Readout efficiency 98 %
- Power budget 2 W/cm²

Architecture

- Analog pixel matrix, digital EoC
- Transmission lines send discriminated hits to EoC
- Data driven, trigger-less
- Data output: 4x 2.4 Gb/s
- IBM CMOS 130 nm, 1.2V, 8 Metal layers



Timing resolution limit of sensor

Timing resolution

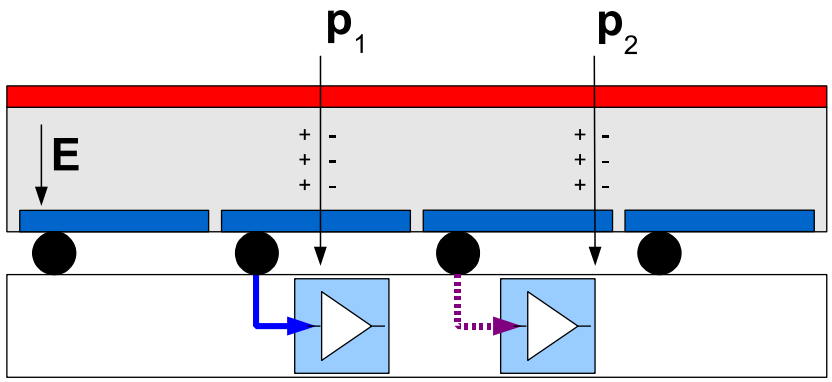
- Laser: 75 ps RMS
- Test beam: 175 ps RMS

Random fluctuations of input current signal shape

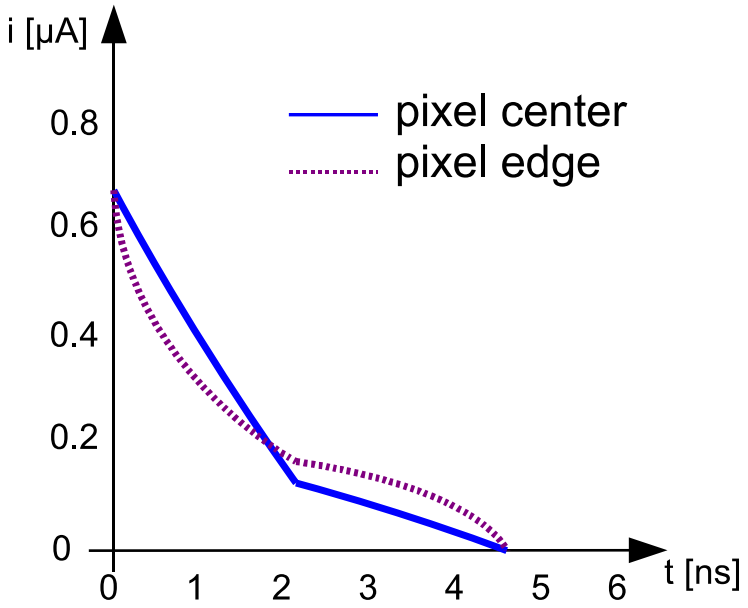
- Position of track hit in pixel
- Charge straggling

Ongoing studies

- Track hit position
  - Position scan with laser: 85 ps RMS
- Charge straggling
  - > 60 ps RMS



Sensor current pulses



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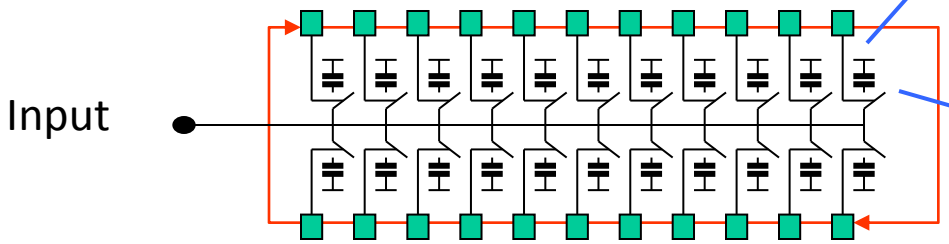
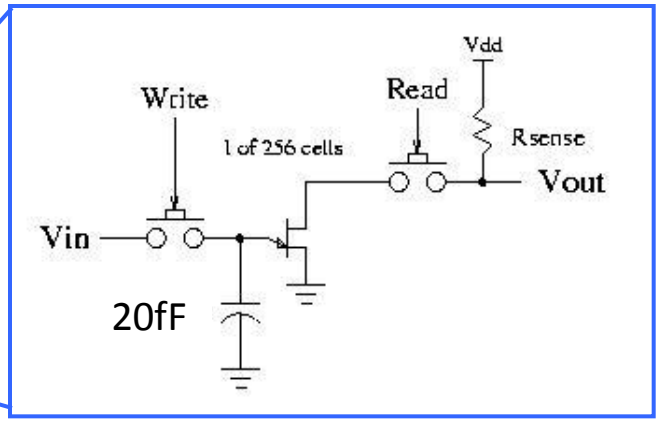
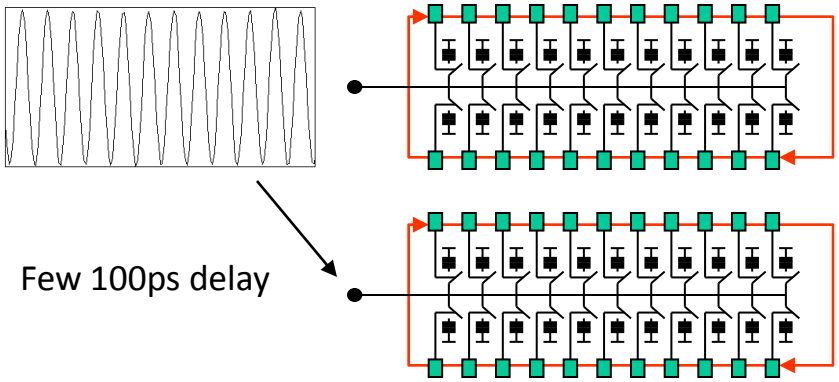
Switched Capacitor Array Sampling

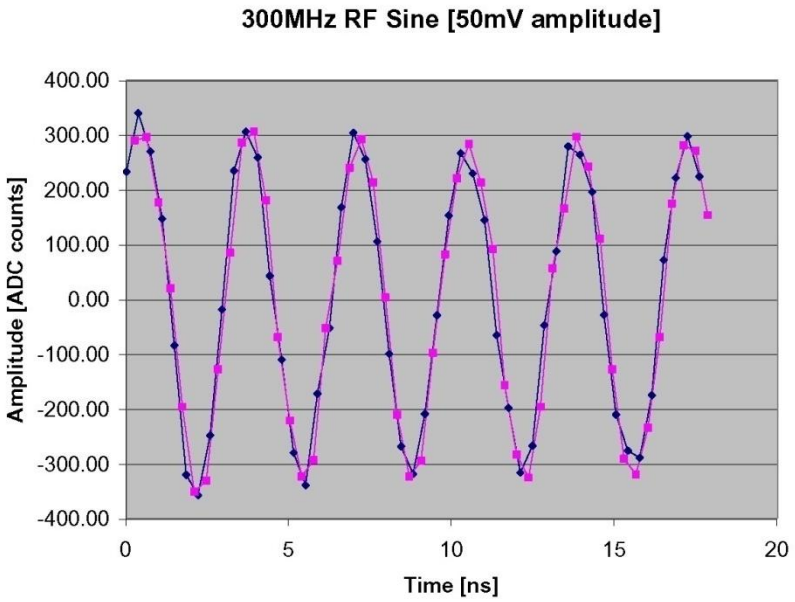
- Write pointer is ~few switches closed @ once





Tiny charge: 1mV ~ 100e$^-$





Now a variety of options…

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

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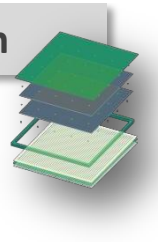
- ✓ E Oberla (University of Chicago): Large area picosecond photodetector collaboration (LAPPD)

LAPPD Collaboration

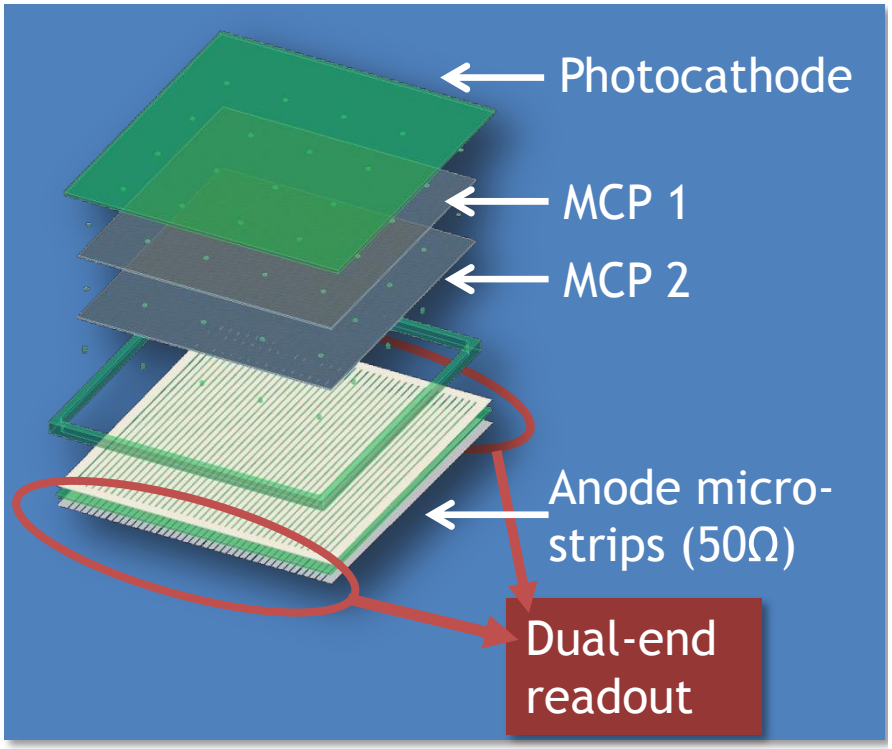


The LAPPD project

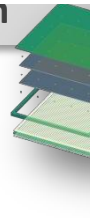
- Development of large-area, relatively inexpensive Micro-Channel Plate (MCP) photo-detectors
  - 8” x 8” tubes = ‘tile’

***Much* more: Saturday 4-6pm, Ballroom 9**

- **“Super Module”:**
  - **2x3 array of 8” tiles**



PSEC-3 + (upcoming) PSEC-4



	PSEC-3		PSEC-4
	SPECIFICATION	**ACTUAL**	**SPEC**
Sampling Rate	500 MS/s-17GS/s	2.5 GSa/s-17GS/s	2.5 GSa/s-17GS/s
# Channels	4	4	6 (or 2)
Sampling Depth	256 cells	256 Cells	256 (or 768) points
Sampling Window	256*(Sampling Rate)$^{-1}$	256*(Sampling Rate)$^{-1}$	Depth*(Sampling Rate)$^{-1}$
Input Noise	1 mV RMS	1-1.5 mV RMS	<1 mV RMS
Dynamic Range	0-1V	0-1V	0-1V
Analog Bandwidth	1.5 GHz	Average 600 MHz	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz	Up to ~10 bit @ 2GHz	Up to 12 bit @ 2GHz
Latency	2 µs (min) – 16 µs (max)	3 µs (min) – 30 µs (max)	2 µs (min) – 16 µs (max)
Internal Trigger	yes	yes	yes

Red= issues addressed from PSEC-3

(Hawaii and Chicago work together)

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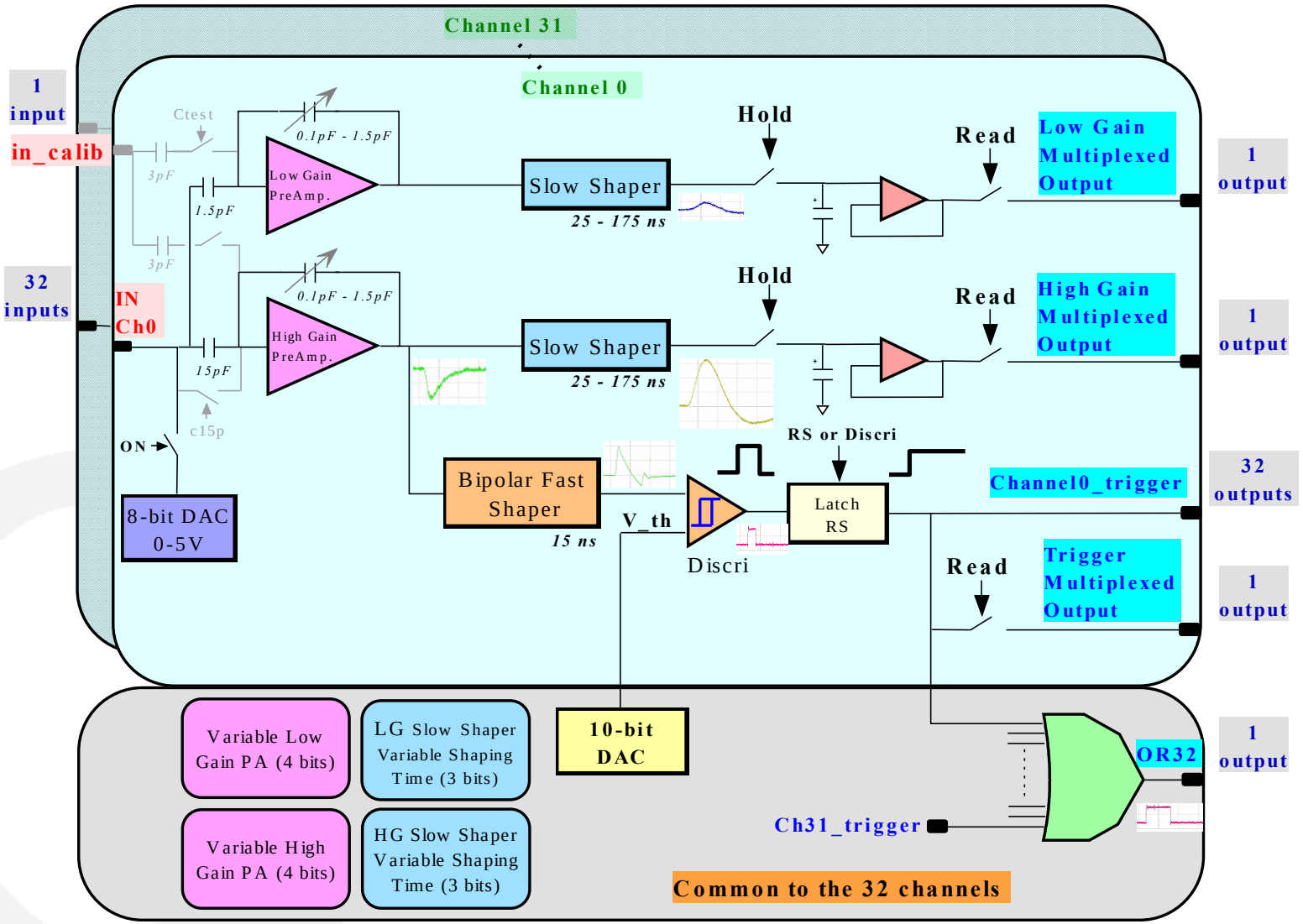
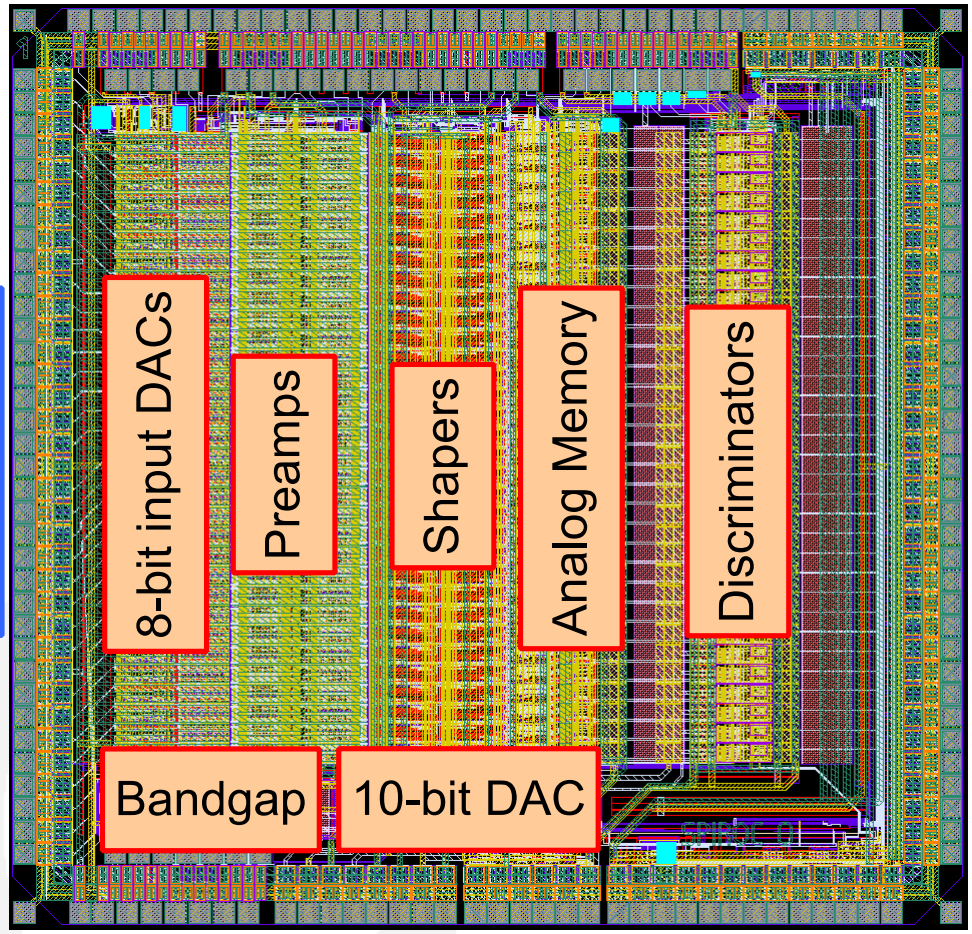
- ✓ Salleh Amhad (IN2P3/OMEGA, France): Spaciroc/Easiroc.Readout ASIC for JEM-EUSO and also for SiPM readout

EASIROC ANALOGUE CORE



EASIROC LAYOUT



Technology :

AMS 0,35µm SiGe

Die size : 16.6mm²

4.157 x 4.013 mm²

Package :

- Naked (PEBS)
- TQFP160

TQFP: heigth=1.4 mm

In a nutshell….

- ✓ Gustavo Cancello (Fermilab): Noise reduction technique using LBNL CCDs. Achieving 0.5e at 50 kpix/s based on estimator for low frequency noise implemented in a FPGA
- ✓ ATLAS Lar Calorimeter: Frontend electronics upgrade for HL LHC: (BNL)
  New IC for the preamp instead of discrete (0.25um SiGe)
  New mixed mode IC to replace DMILL
  ATCA based readout out…