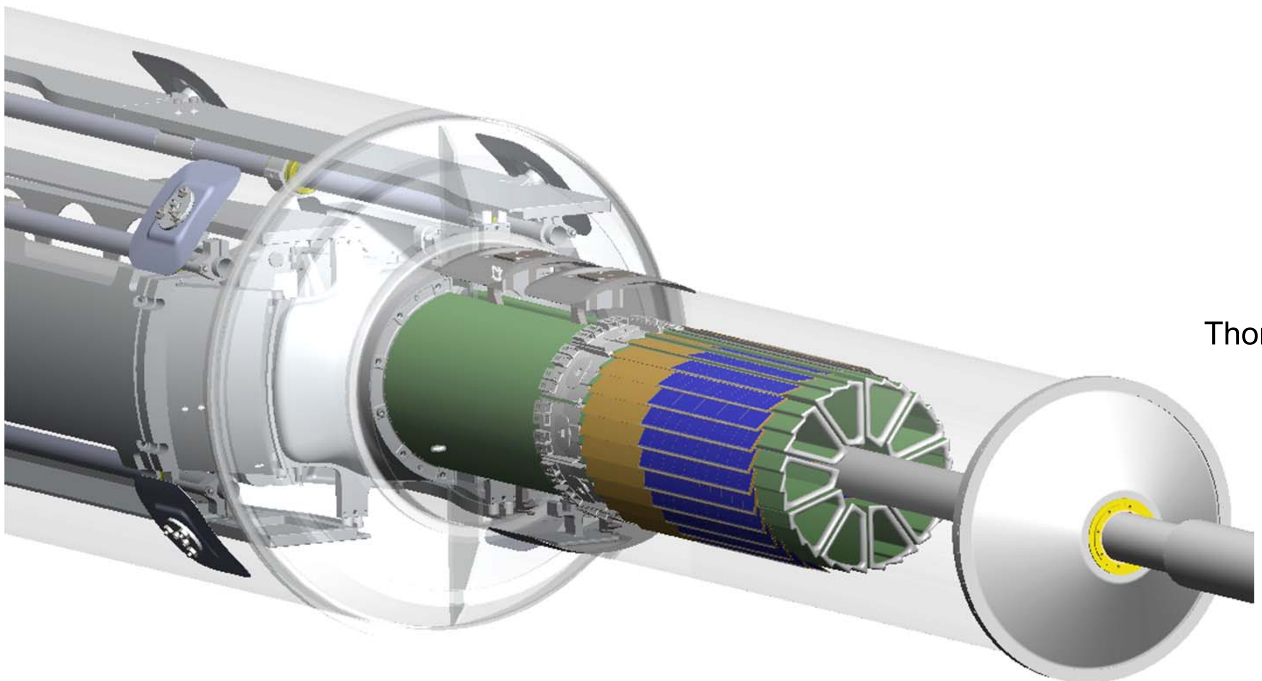
# A MAPS based pixel vertex detector for the STAR experiment

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# Talk Outline



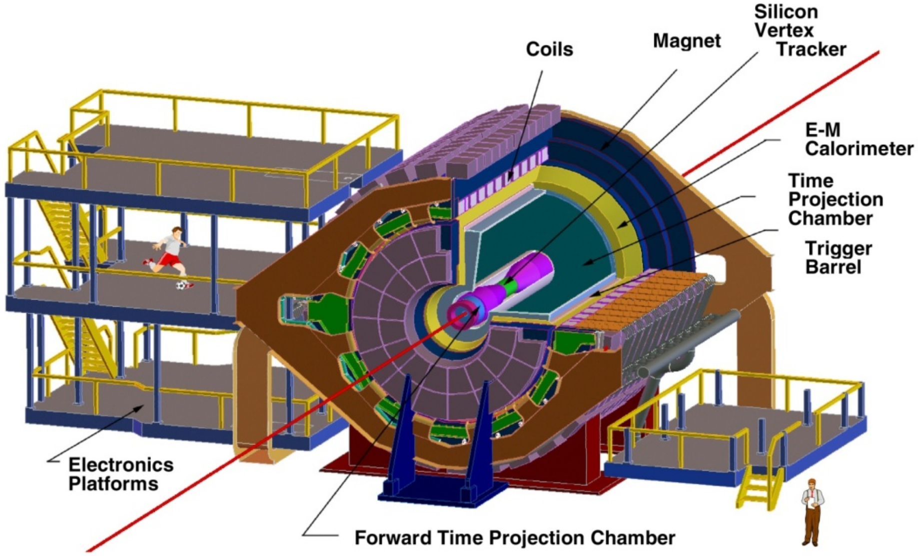
The primary focus of this talk is technical and on instrumentation.

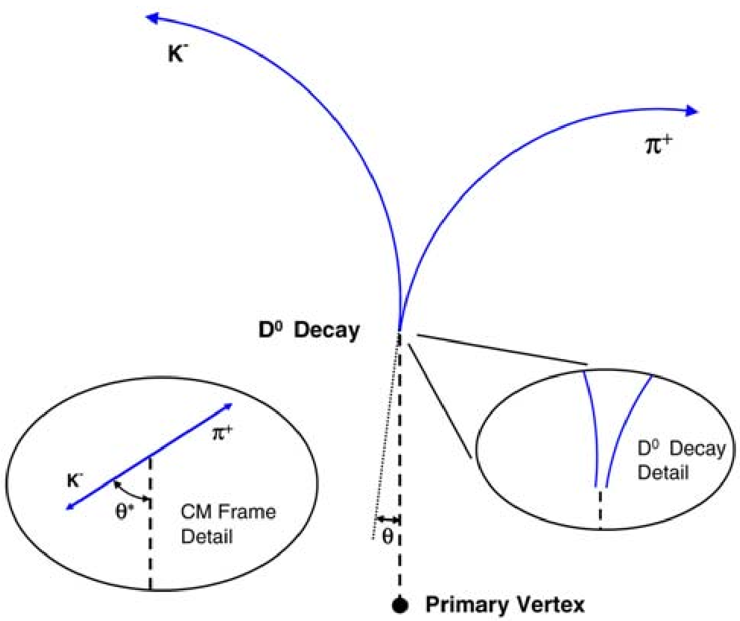
- STAR detector upgrades at RHIC.
- Pixel detector requirements, design and characteristics.
- Detector development and prototyping flow path and status.
  - o Emphasis on sensors and ladders
- Summary and plans.

# Vertex Detector Motivation

STAR HFT

## Upgrades to the STAR Detector at RHIC



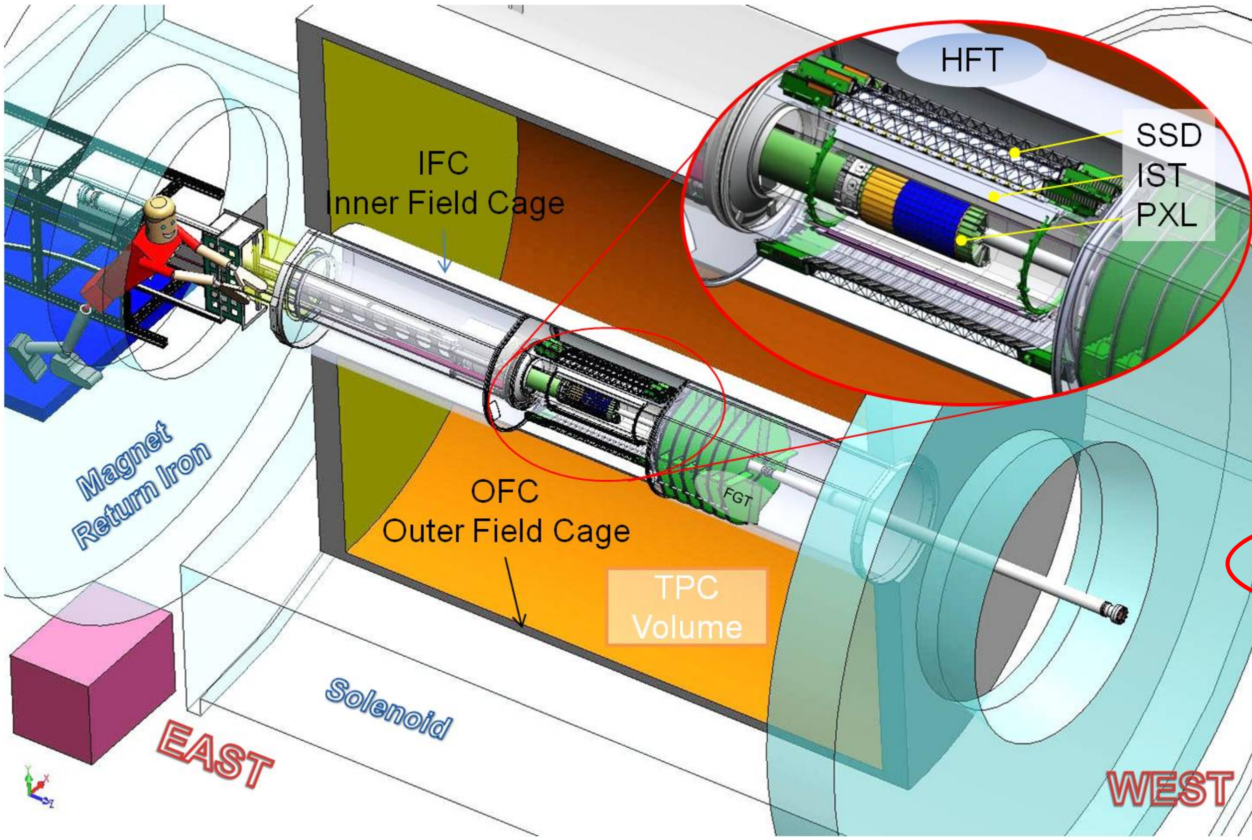




Direct topological reconstruction of Charm

Detect charm decays with small $c\tau$, including $D^0 \rightarrow K + \pi$

Method: Resolve displaced vertices (100-150 microns)

# PXL in Inner Detector Upgrades




TPC – Time Projection Chamber (main tracking detector in STAR)

*HFT – Heavy Flavor Tracker*

- SSD – Silicon Strip Detector
  - r = 22 cm
- IST – Inner Silicon Tracker
  - r = 14 cm
- PXL – Pixel Detector
  - r = 2.5, 8 cm

We track inward from the TPC with graded resolution:

TPC →(~1mm) SSD →(~300µm) IST →(~250µm) PXL →(<30µm) vertex

# PXL Detector Requirements and Design Choices

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**Requirements**

- $-1 \le \text{Eta} \le 1$, full Phi coverage (TPC coverage)
- ≤ 40 μm DCA pointing resolution required for 750 MeV/c kaon
  - Two or more layers with a separation of > 5 cm.
  - Pixel size of ≤ 30 μm
  - Radiation length as low as possible but should be ≤ 0.5% / layer (including support structure). The goal is 0.37% / layer
- Integration time of < 200 μs
- Sensor efficiency ≥ 99% with accidental rate $\le 10^{-4}$.
- Survive radiation environment.
- Upgrade detector – fit into existing STAR infrastructure (trigger, DAQ, etc.)

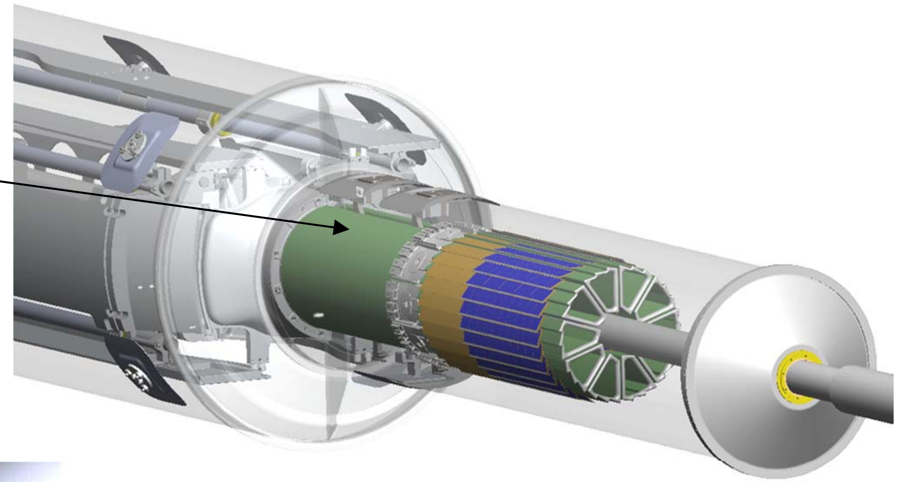
**Design Choices**

- Air cooling
- Thinned silicon sensors (50 μm thickness)
- MAPS (Monolithic Active Pixel Sensor) pixel technology
  - Sensor power dissipation ~170 $mW/cm^2$
  - Sensor integration time <200 μs ($L=8\times10^{27}$)
- Quick extraction and detector replacement (1 day)

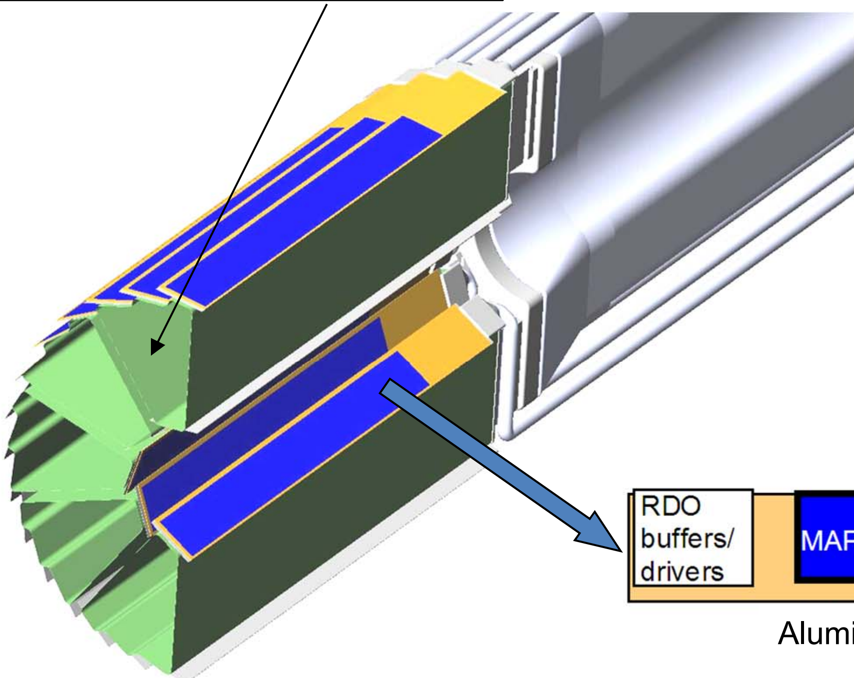
# PXL Detector Mechanical Design



Mechanical support with kinematic mounts (insertion side)

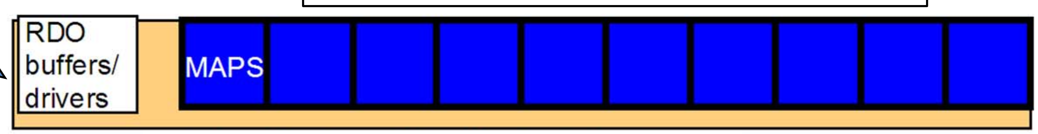


carbon fiber sector tubes (~ 200 μm thick)



**Insertion from one side**
**2 layers**
**5 sectors / half (10 sectors total)**
**4 ladders/sector**

Ladder with 10 MAPS sensors (~ 2×2 cm each)




Aluminum conductor Ladder Flex Cable

20 cm

# PXL Detector Basic Unit (RDO)

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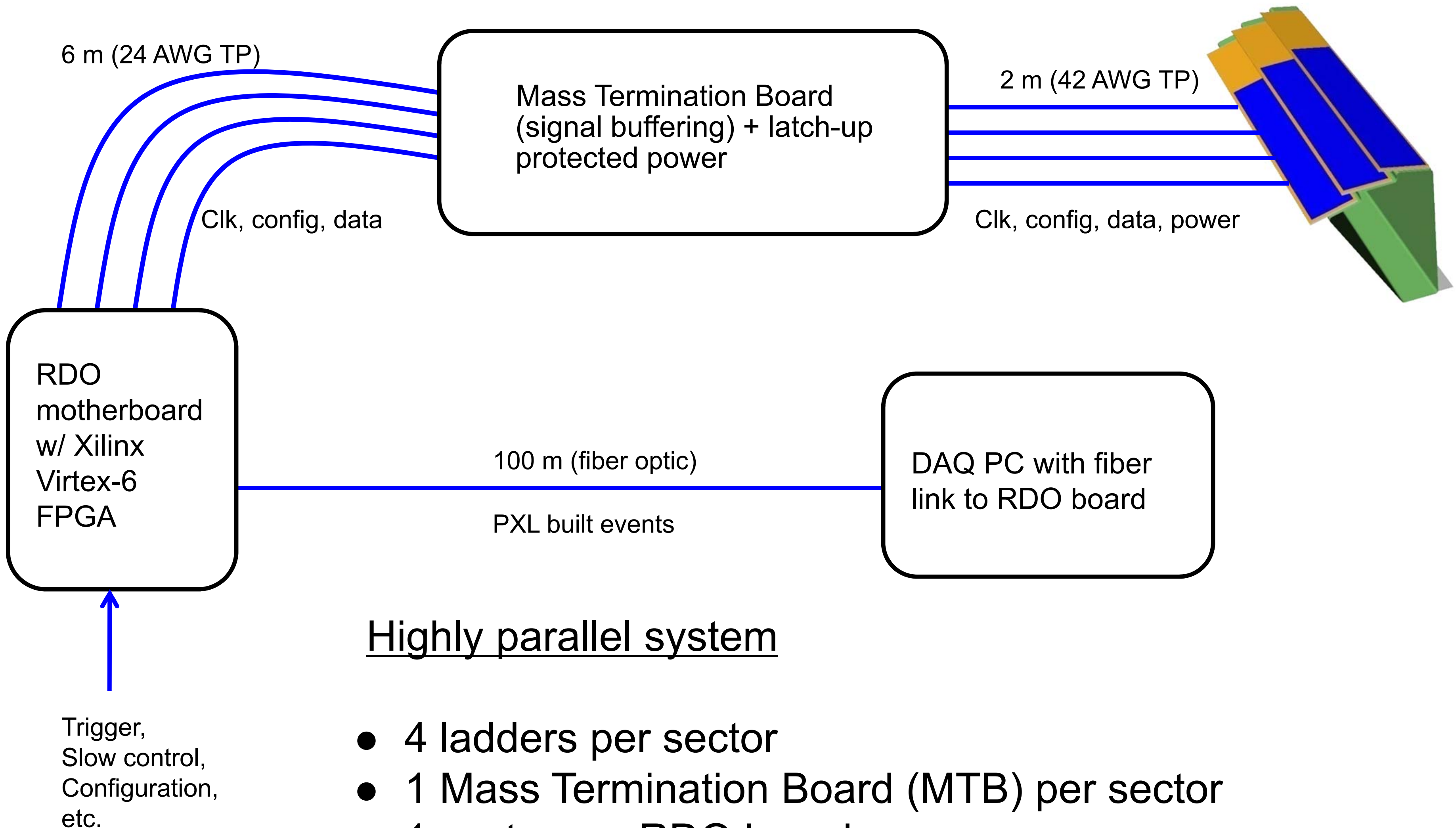


## Highly parallel system

- 4 ladders per sector
- 1 Mass Termination Board (MTB) per sector
- 1 sector per RDO board
- 10 RDO boards in the PXL system

# Detector Characteristics

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| | |
|---|---|
| Pointing resolution | $(12 \oplus 19\ \text{GeV}/p \cdot c)\ \mu m$ |
| Layers | Layer 1 at 2.5 cm radius<br>Layer 2 at 8 cm radius |
| Pixel size | $20.7\ \mu m \times 20.7\ \mu m$ |
| Hit resolution | $6\ \mu m$ |
| Position stability | $6\ \mu m$ rms ($20\ \mu m$ envelope) |
| Radiation length per layer | $X/X_0 = 0.37\%$ |
| Number of pixels | 356 M |
| Integration time (affects pileup) | 185.6 $\mu s$ (occupancy ~250 hits/sensor on inner sensors, ~60 hits/sensor on outer sensors) |
| Radiation environment | 20 to 90 kRad<br>$2 \cdot 10^{11}$ to $10^{12}$ 1MeV n eq/cm$^2$ |
| Rapid detector replacement | ~ 1 day |

356 M pixels on ~0.16 m$^2$ of Silicon

# PXL Detector Production Path (post CD – 2/3)

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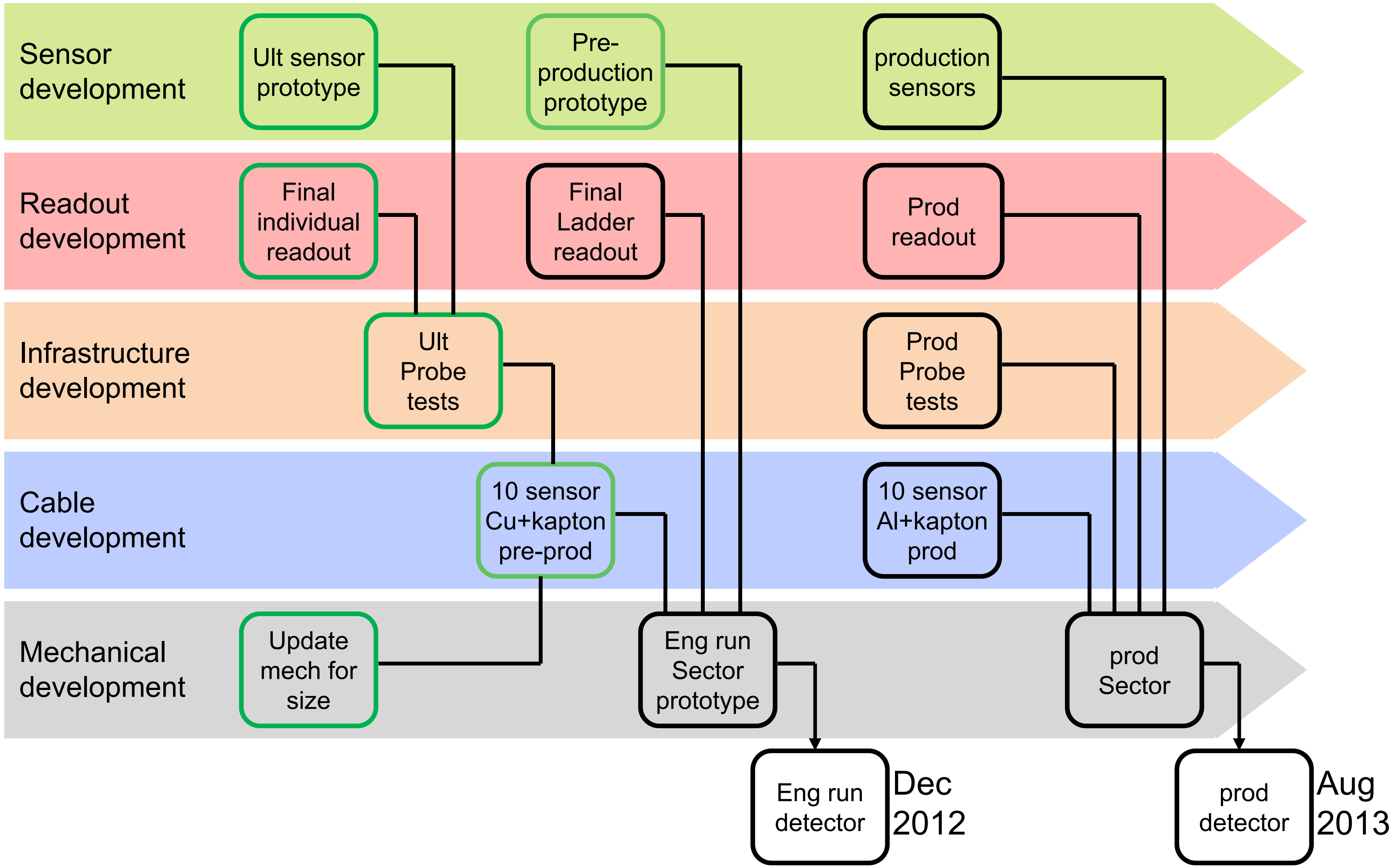
## Culmination of 5 years of development



# PXL Sensor Design

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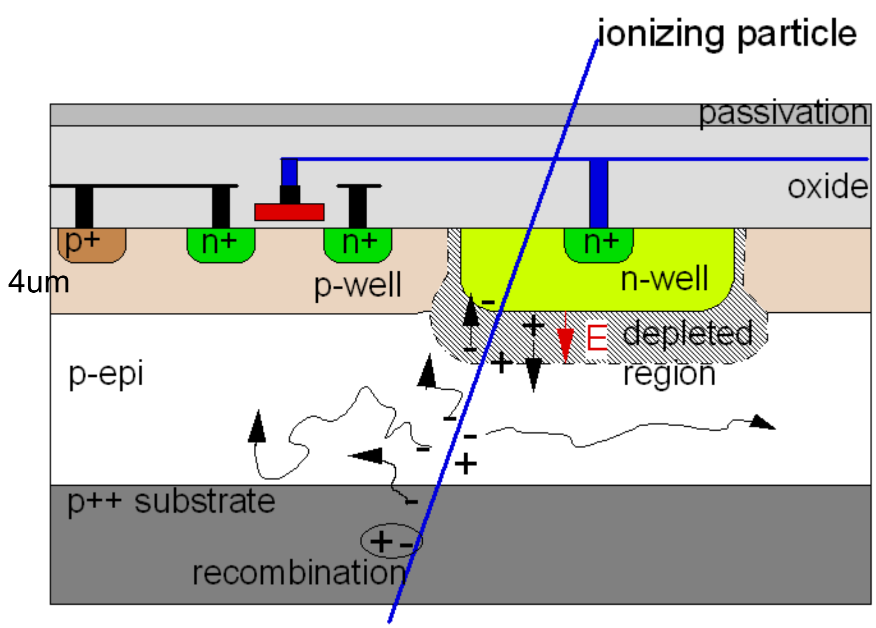
Sensor development → Ult sensor prototype → Pre-production prototype → production sensors

## Monolithic Active Pixel Sensors

MAPS pixel cross-section (not to scale)

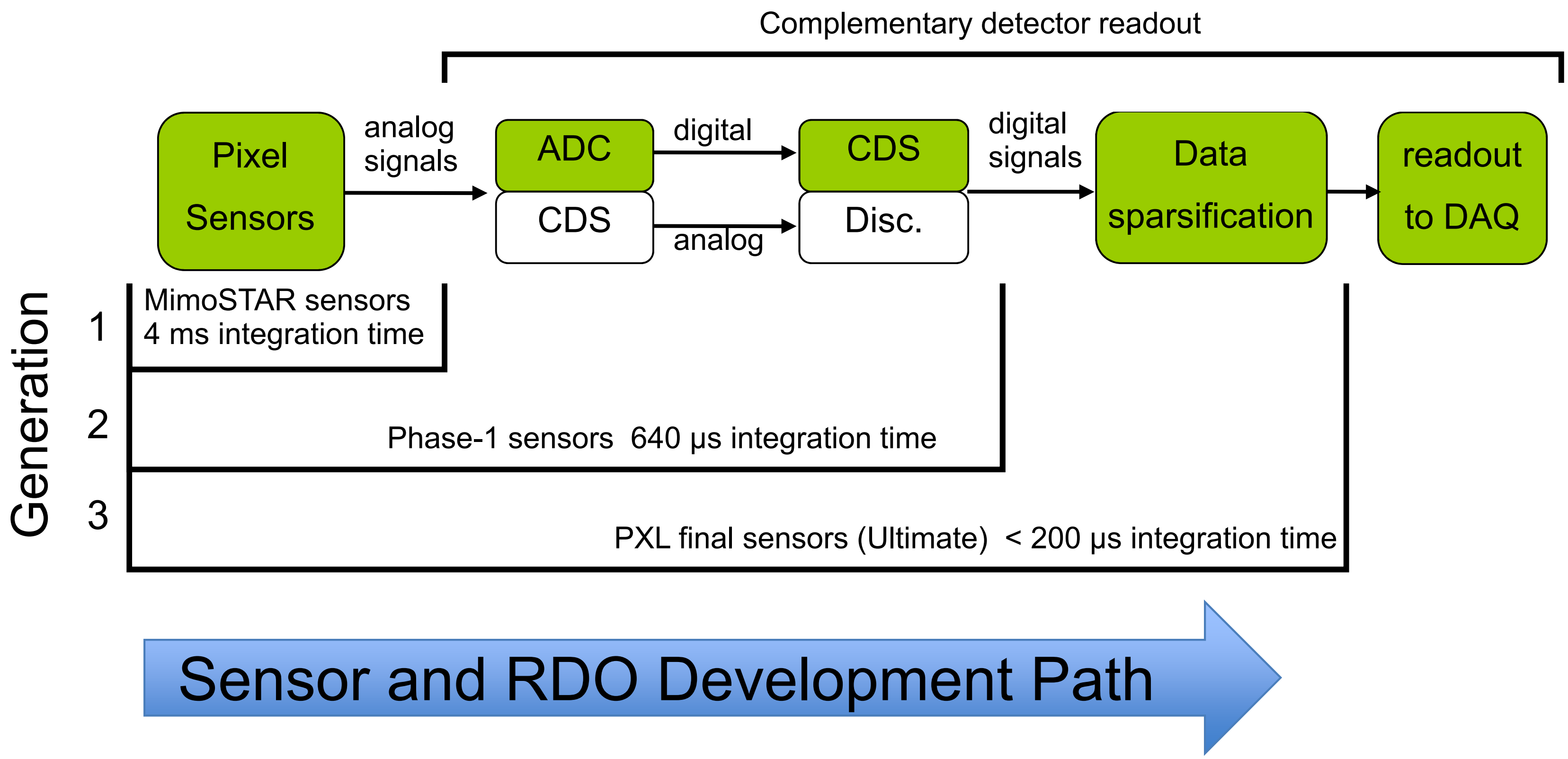



- Standard commercial CMOS technology (AMS-C35B4/OPTO uses 4 metal- and 2 poly- layers.)
- Room temperature operation
- Sensor and signal processing are integrated in the same silicon wafer
- Signal is created in the low-doped epitaxial layer (typically ~10-15 μm) → MIP signal is limited to <1000 electrons
- Charge collection is mainly through thermal diffusion (~100 ns), reflective boundaries at p-well and substrate.
- 100% fill-factor
- Fast readout
- Proven thinning to 50 micron

# Sensor generation and RDO attributes



Develop sensor chips, 3 generation program
Sensors are designed by Marc Winter's group at IPHC.



# Pixel operation and signal extraction

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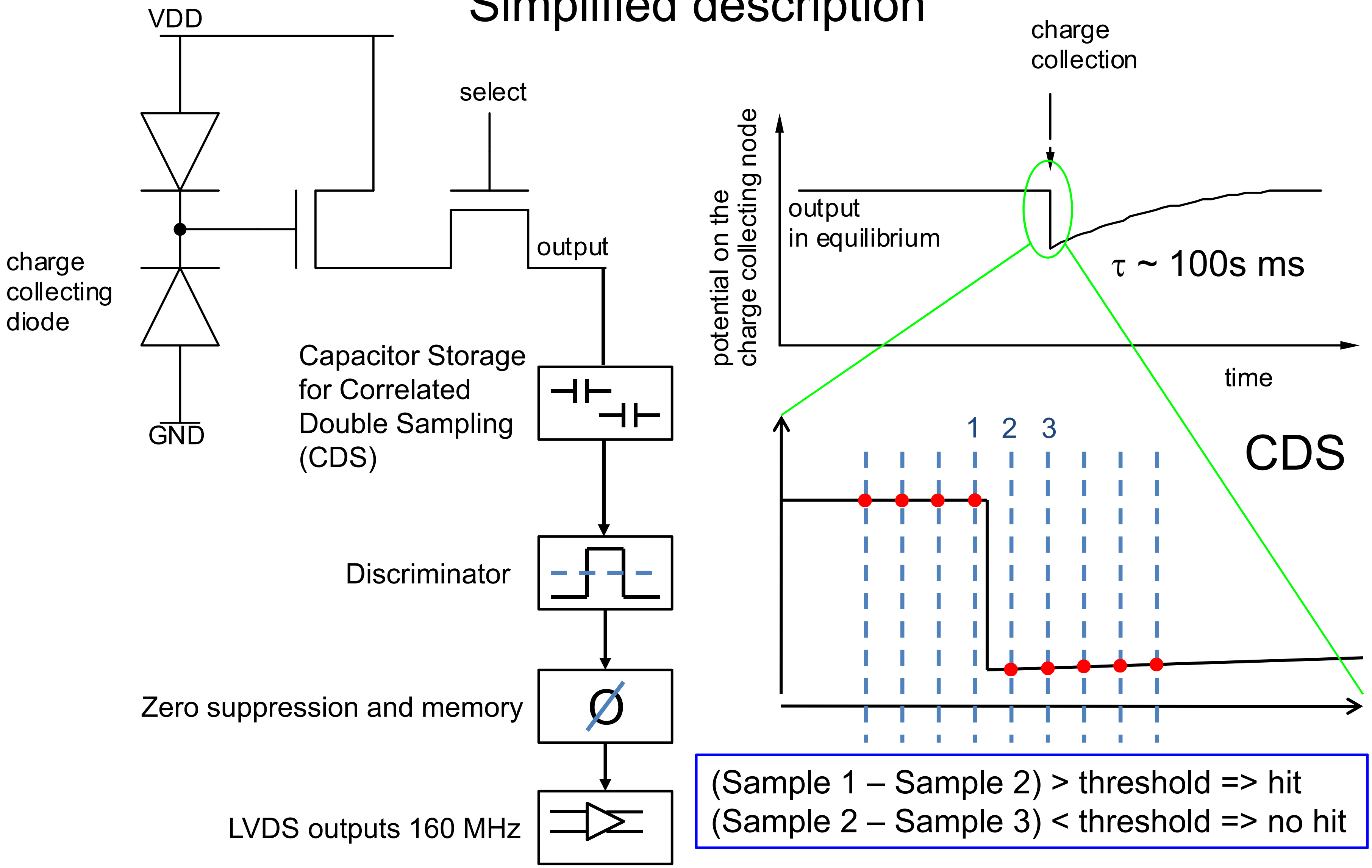
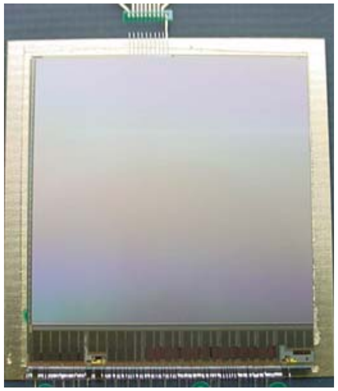
## Simplified description

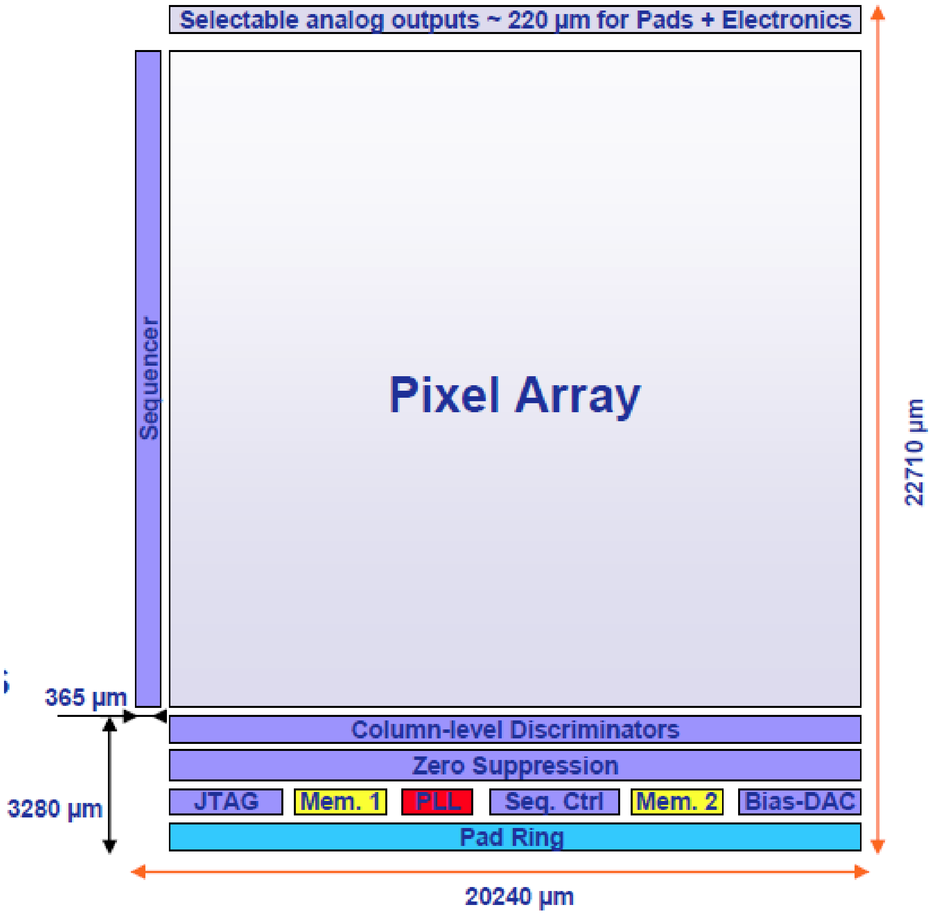



(Sample 1 – Sample 2) > threshold => hit
(Sample 2 – Sample 3) < threshold => no hit

# PXL detector Ult -1 prototype








- Reticle size (~ 4 cm²)
  - Pixel pitch 20.7 µm
  - 928 x 960 array ~890 k pixels
- Power dissipation ~170 mW/cm² @ 3.3V
- Short integration time 185.6 µs
- on-chip CDS, column level discriminators and zero suppression
- 2 LVDS data outputs @ 160 MHz
- Run length encoding on rows with up to 9 hits/row.
- Ping-pong memory for frame readout (~1000 hits deep)
- High Res Si option – significantly increases S/N and radiation tolerance.

# Ultimate 1 efficiency vs. fake hit rate

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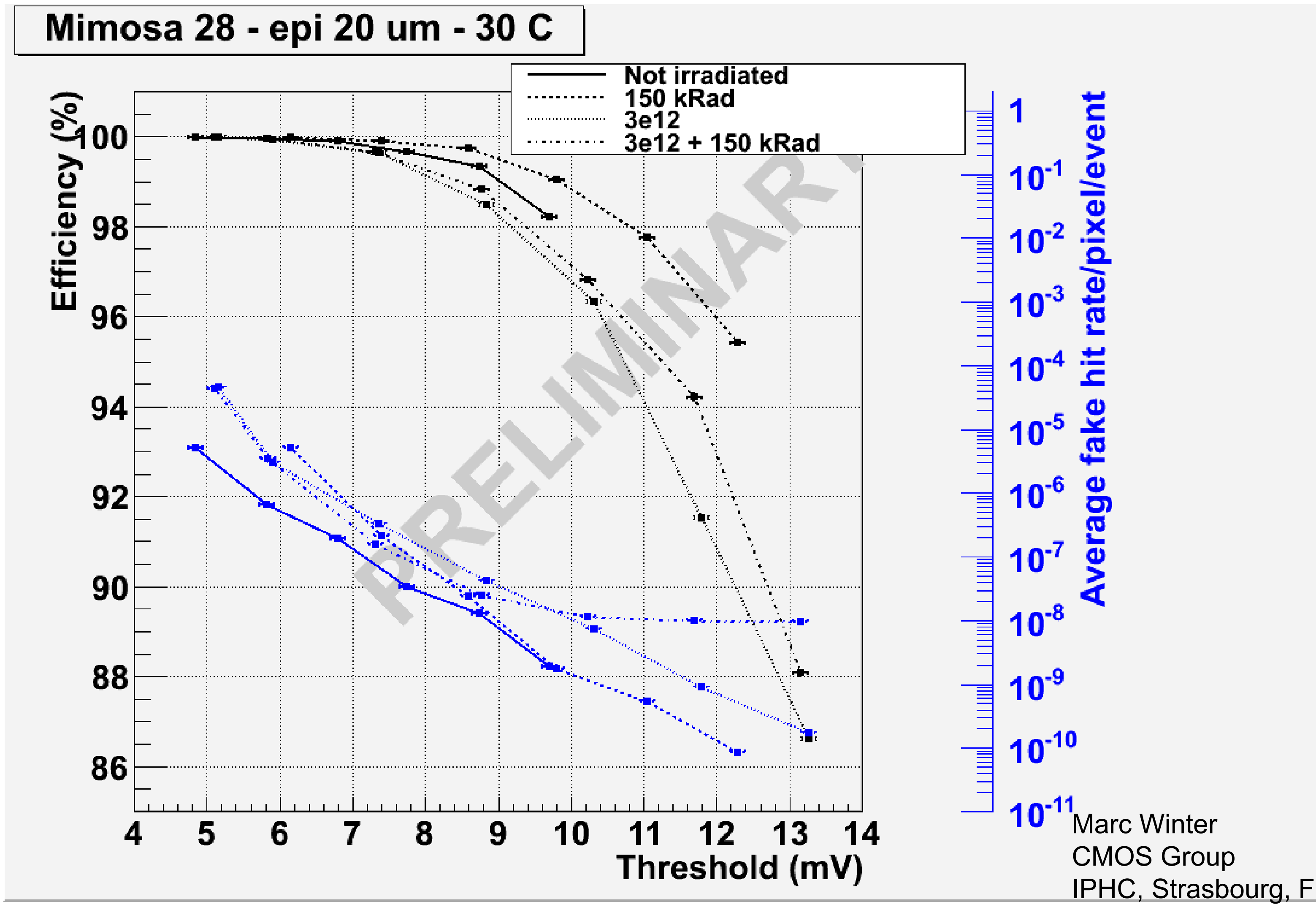



Marc Winter
CMOS Group
IPHC, Strasbourg, France

Developed and tested by IPHC

# PXL Sensor Status



Sensor development → Ult sensor prototype → Pre-production prototype → production sensors

- Prototype PXL sensors (Ultimate 1) were tested at CERN test beam facility using a prototype PXL RDO system. The IPHC measured efficiency and accidental rate were reproduced. The sensors are functionally acceptable for engineering run use.
- Next generation Ultimate 2 has been submitted for fabrication (minor fixes and improvements).
- We have procured, diced and thinned 11 wafers of Ultimate 1 sensors. The mechanical dicing / thinning yield was 93%. These sensors will be used for the engineering run detector.

# Probe Testing Development

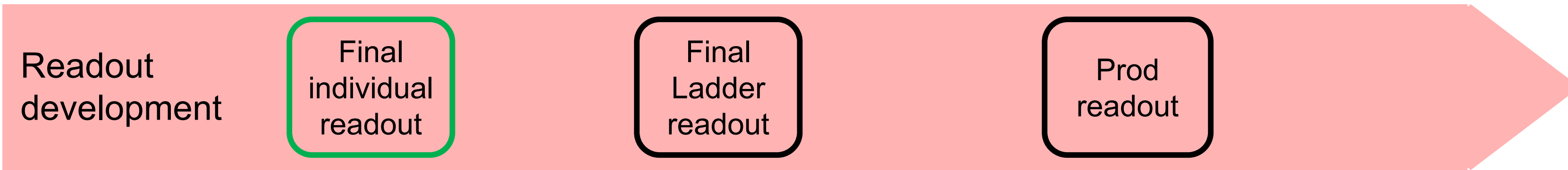


Infrastructure development → Prototype Probe tests → Final Probe tests

- Yield modeling shows probe testing to be critical to the goal of assembling functional 10 sensor ladders.
- We will be performing automated testing of thinned 50µm (curved) sensors on custom vacuum chuck carriers.

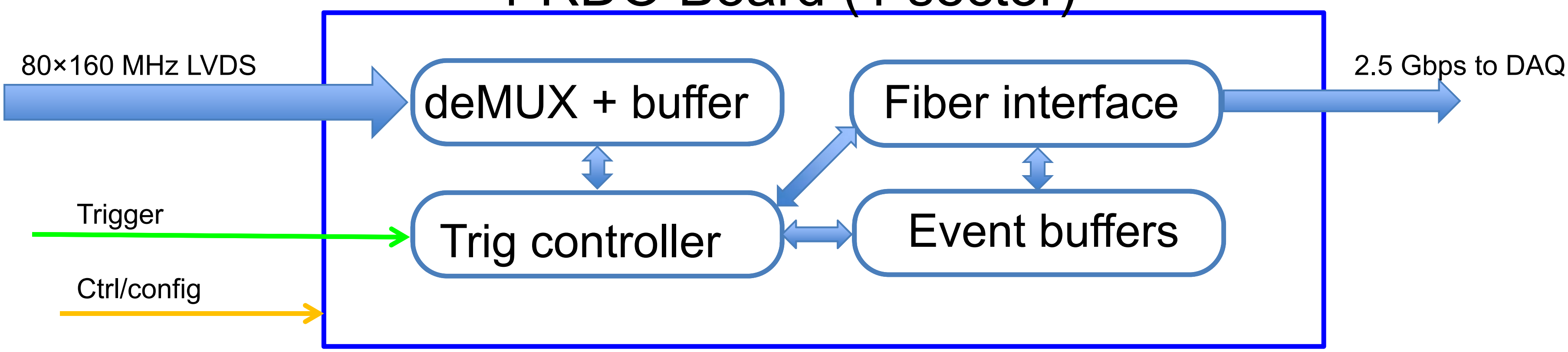
- We have a functioning probe testing system for the Ultimate 1 sensors. The system includes a vacuum chuck for 20 thinned sensors.
- We do full sensor testing and characterization using the full RDO system. (JTAG, 160MHz LVDS data RDO) This allows us to obtain initial bias and threshold settings to be used in beam.
- Scripted probe testing is functional. The final interface to the database is underway.

# Read-out Electronics




1. The detector RDO structure is highly parallel with 10 identical detector sector / RDO chains.
2. Each sector is configured and delivers data to the RDO boards continuously into a data pipeline.
3. The receipt of a trigger opens an event buffer for 1 frame of data.
4. The frame(s) data is sorted, formed into an event and shipped to the DAQ receiver PCs.

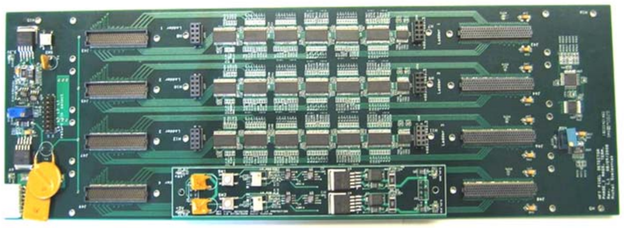
## 1 RDO Board (1 sector)



# Read-out Electronics



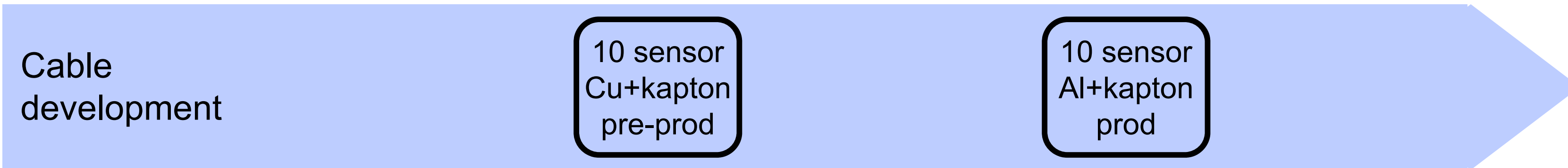
Pre-production motherboard in 9U VME mechanical standard. Processing is accomplished using a Xilinx Virtex-6 FPGA. The RDO for the full 356M pixel detector resides in one 9U VME crate.



Prototype Mass Termination Board

Individual sensor internal raw data rate = 600 MB / s
Raw data rate / sector (max) = 1.6 GB / s
Data rate / sector saved (1kHz trigger) = 23 MB / s

# Cable Development

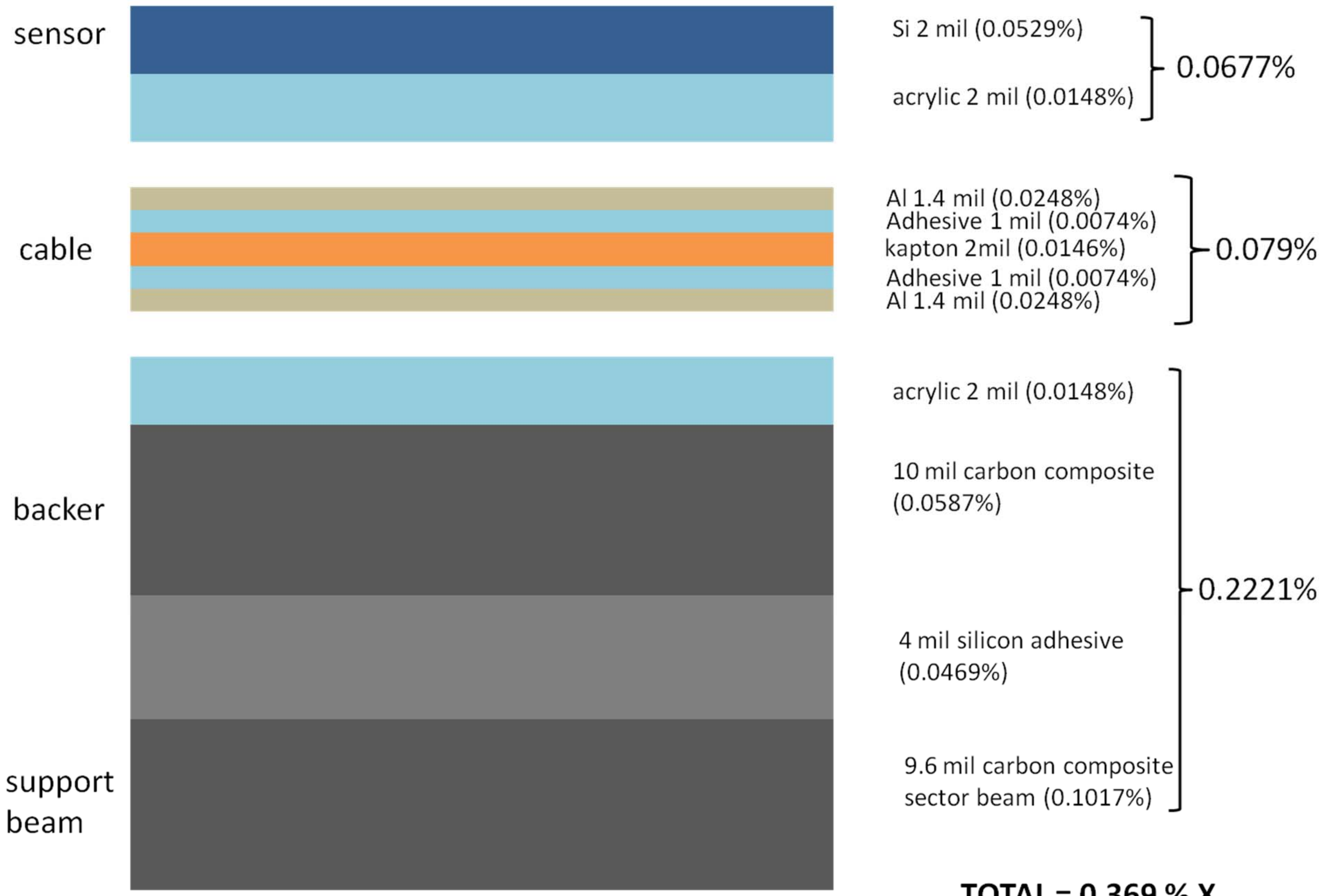



- The cable is needed to deliver power and ground and provide signal routing to and from the sensors on the ladder with minimal radiation length (material).
- Production aluminum conductor flex cables will be fabricated in the CERN PCB shop.

Hybrid Copper / Aluminum conductor flex cable
Preliminary design concept


Low mass region calculated $X/X_0$ for Al conductor = 0.079 %
Low mass region calculated $X/X_0$ for Cu conductor = 0.232 %

# Radiation Length of active area




**TOTAL = 0.369 % $X_0$**

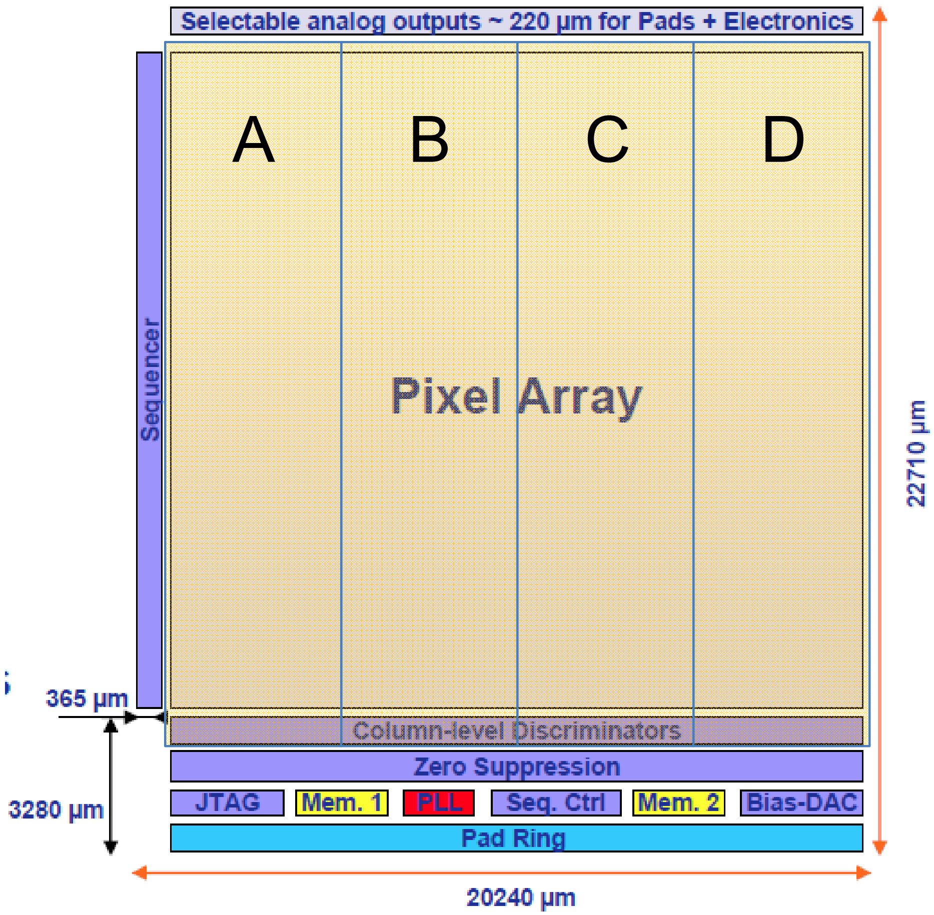
NOTE: Does not include sector tube side walls

# Cable Development

Correct form factor cable prototype with 10 × 50 µm Ultimate 1 sensors.

- Prototype cable has been tested and is fully functional with low crosstalk / noise increase compared to single sensor operation.
- Pre-production version in kapton + Cu conductor being fabricated in CERN PCB shops for use in the engineering run detector. Some kapton + Al conductor will also be fabricated for testing and validation.

# Sensors on ladders




- Sensor is divided into 4 sub-arrays of 240 columns each.
- Each sub-array has a single threshold value applied to all columns in the sub-array.
- We test at 3 supply voltages (3.3V, 3.0V 2.9V)

# Examples of failures

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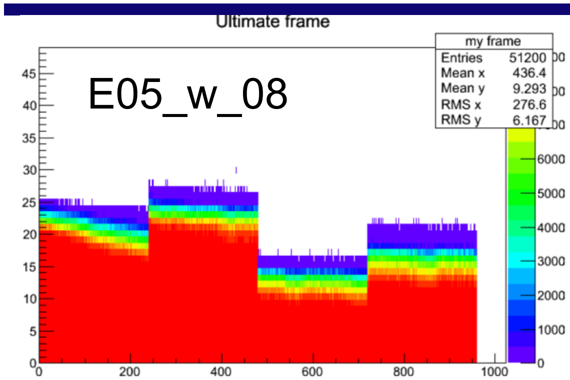
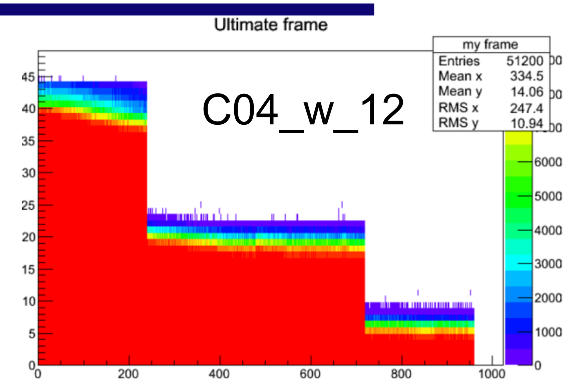
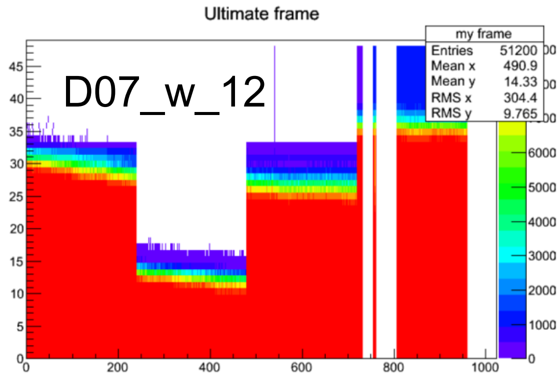


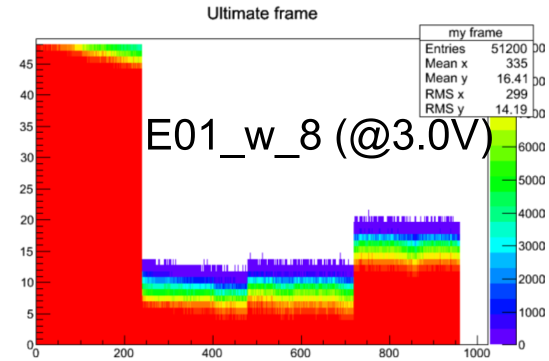

OK

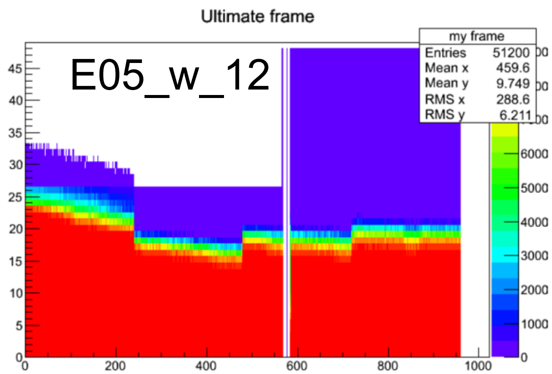



Faulty columns

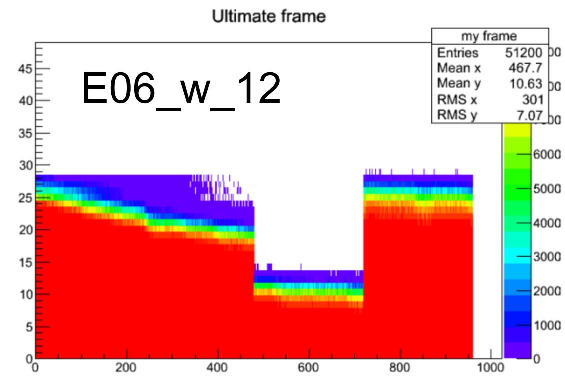
Sub-arrays




Faulty rows

3.3 or 3.0 V



# Ladder L1 measured noise

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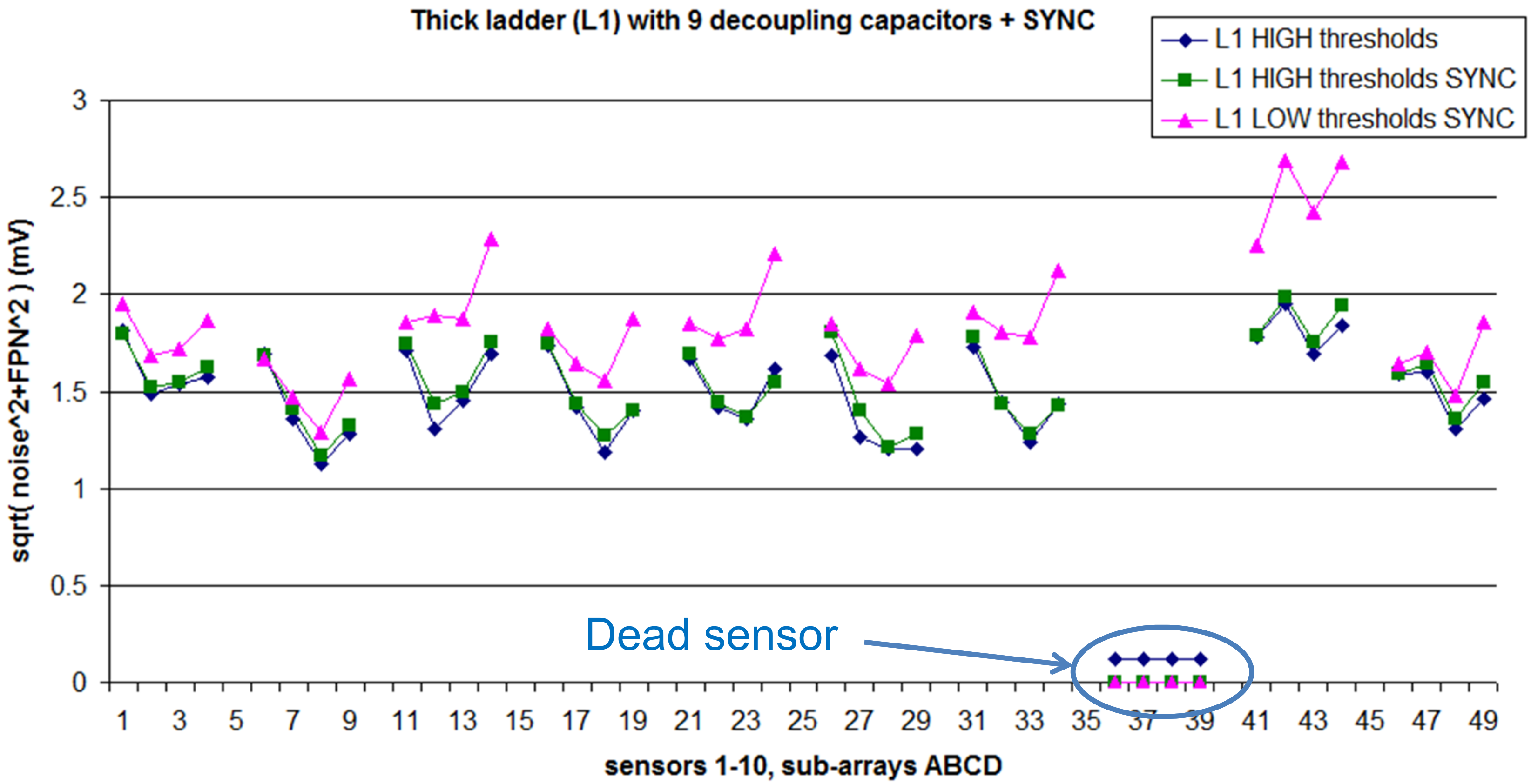



- High thresholds ~ standard operating condition (60-250 hit occupancy)
- Low thresholds ~ worst possible operating condition (full output activity – overflow on memories)

# PXL Mechanical



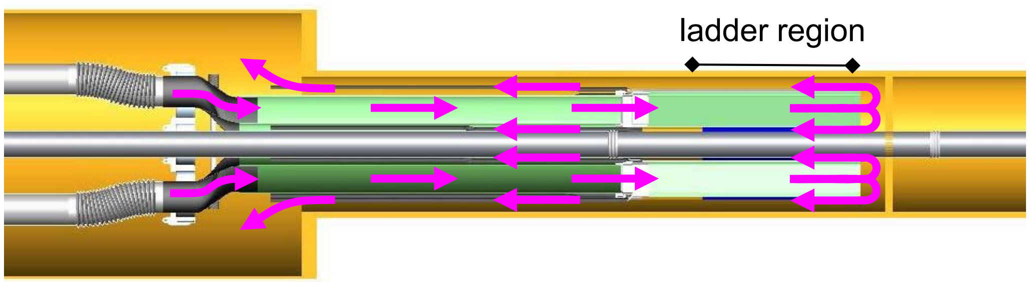
| Mechanical development | Update mech for size | Eng run Sector prototype | prod Sector |
|---|---|---|---|

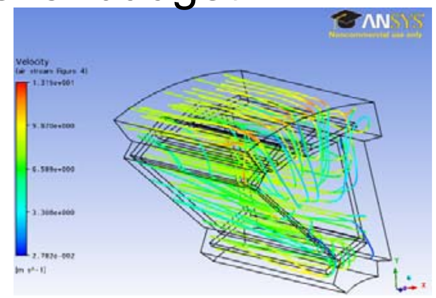
- Meeting the stability requirement is a challenge (20μm)
- The full PXL mechanical design, tooling, fixturing and insertion mechanism are implemented in solid modeling CAD.
- Thermal distortion, vibration, and cooling simulations are complete.
- Mechanical test sectors have been assembled using the tooling and used for thermal and vibration testing.
- The thermal and vibration simulations have been verified on a mechanical model of the detector.

# Mechanical Development

STAR HFT

Air-flow based cooling system for PXL to minimize material budget.

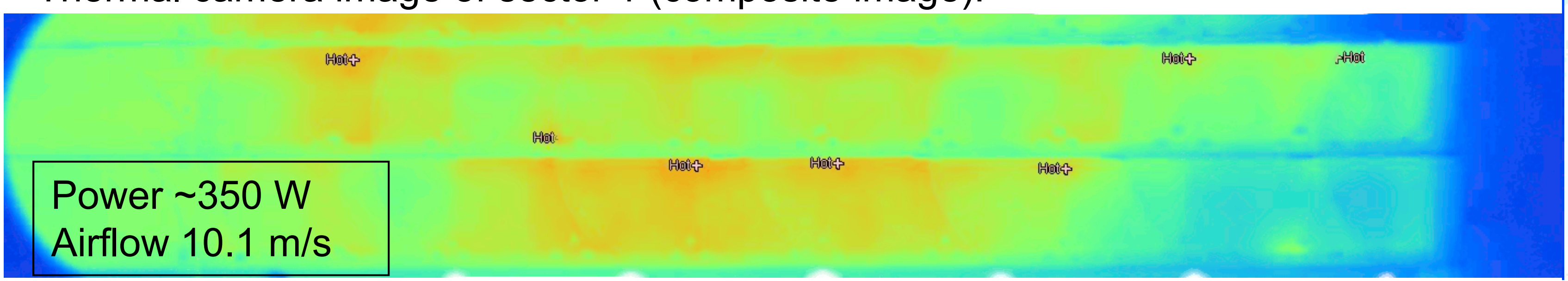


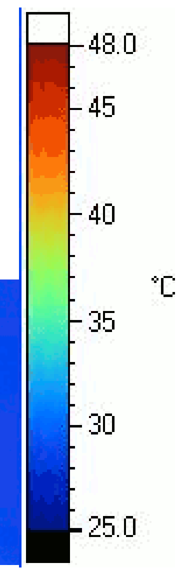




computational fluid dynamics simulation


- Silicon power: tested at 170 $mW/cm^2$ (~ power of sunlight)
- 350 W total in the ladder region (Si + drivers)
- At 10 m/s airflow ΔT is kept to ~10º C
- Vibration and translation is within acceptable limits.

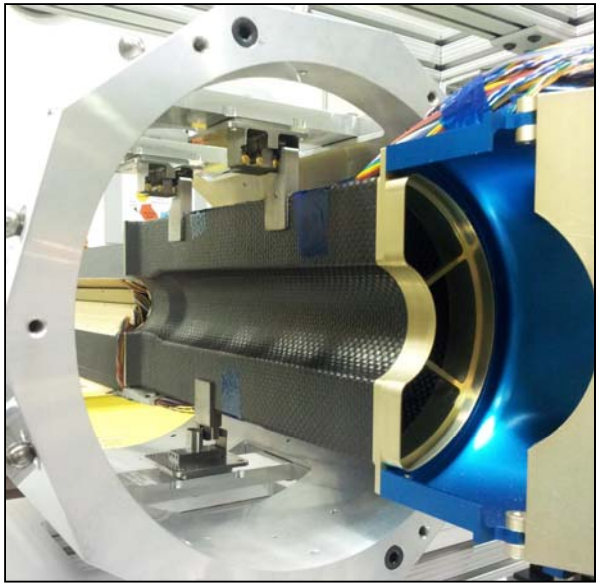
Thermal camera image of sector 1 (composite image):

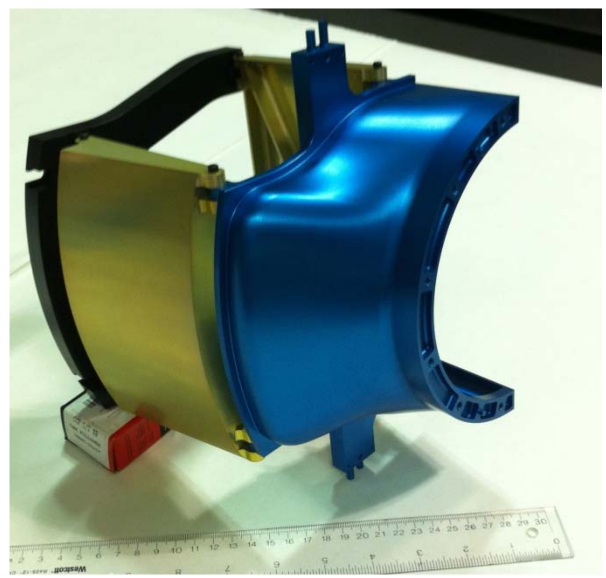


# Mechanical Development







# 1.2.1 PXL Mechanical



| Mechanical development | Update mech for size | Eng run Sector prototype | prod Sector |
|---|---|---|---|

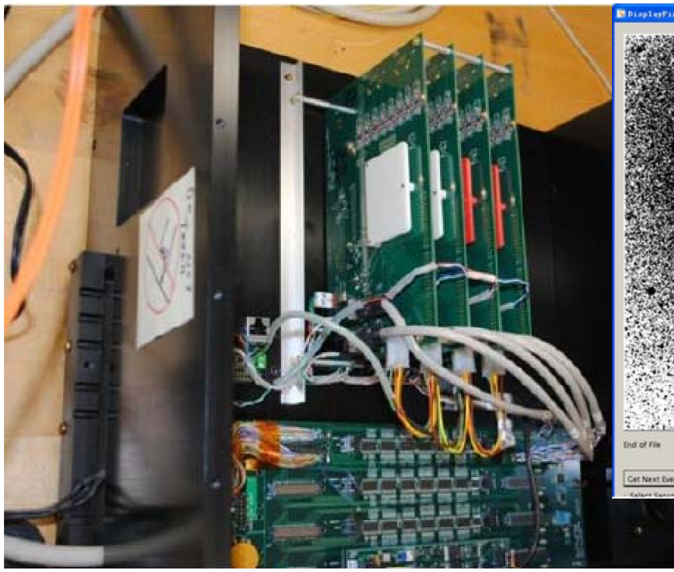
- Most major PXL components are fabricated or in process. Full insertion and kinematic mount testing is now complete and the mechanical design is functional and has (thus far) met the required level of stability.
- The inner detector support system (CFC shells and mounts) have been fabricated and will be installed into the STAR detector in the next few weeks together with the new small radius beam pipe.

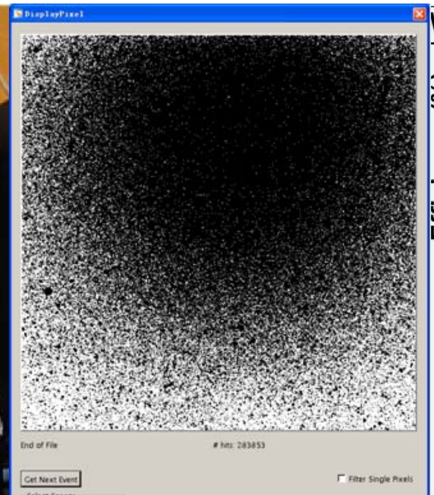
# Summary and plans



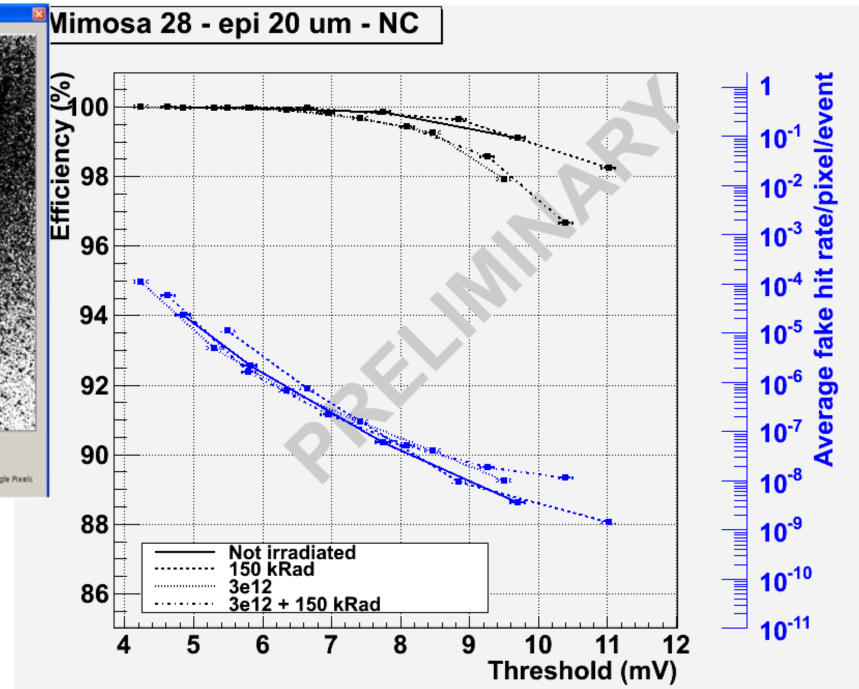
- The HFT upgrade for STAR is well advanced in design, we passed our DOE CD-2/3 review in September 2011 and full ladder production is beginning.
- The PXL detector simulations and prototyping indicate that we should be able to achieve a new standard in low radiation length vertex detectors.
- The STAR PXL detector will be the first MAPS based vertex detector used at a collider accelerator experiment.
- We expect to produce a several sector prototype detector for installation in the December 2012 run.
- The final PXL detector along with the rest of the HFT upgrades will be installed for the November 2013 run.

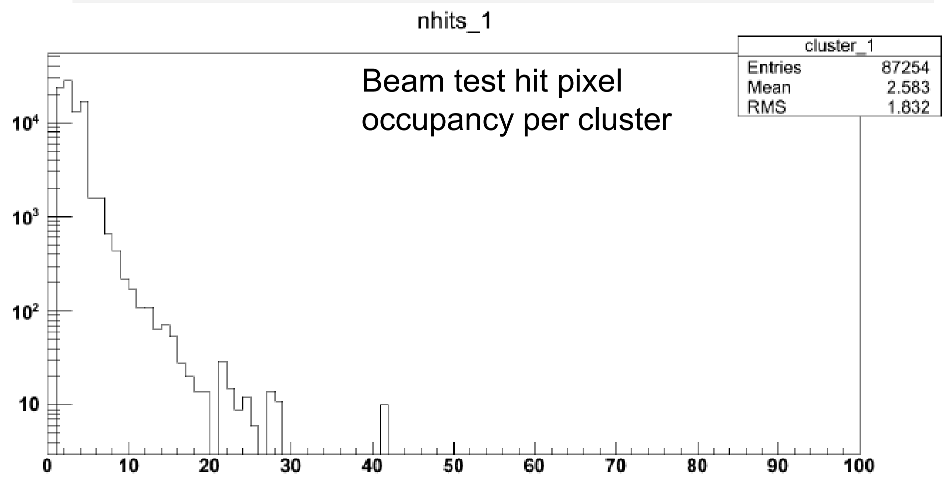
- end





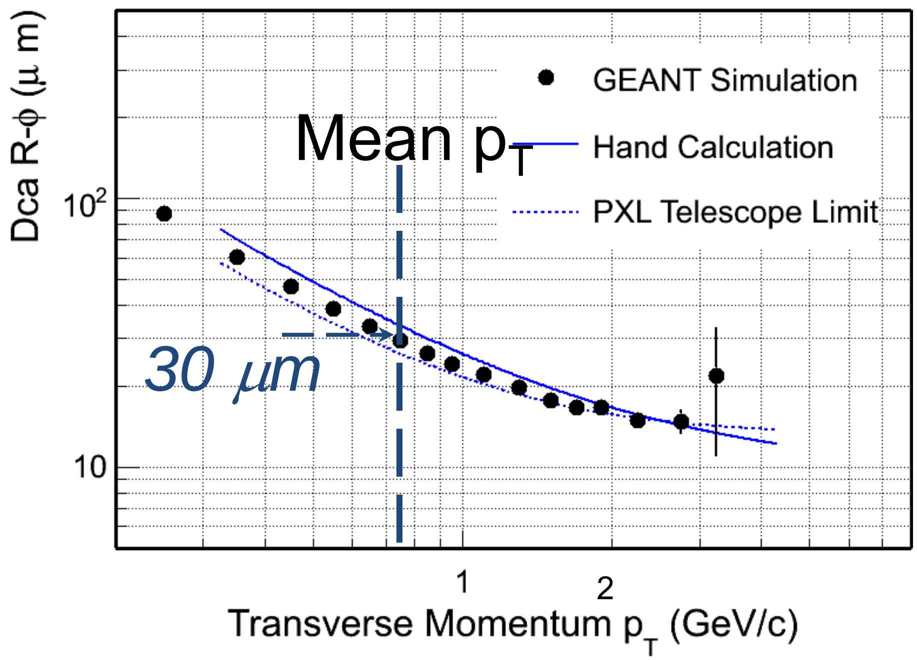

50k triggers

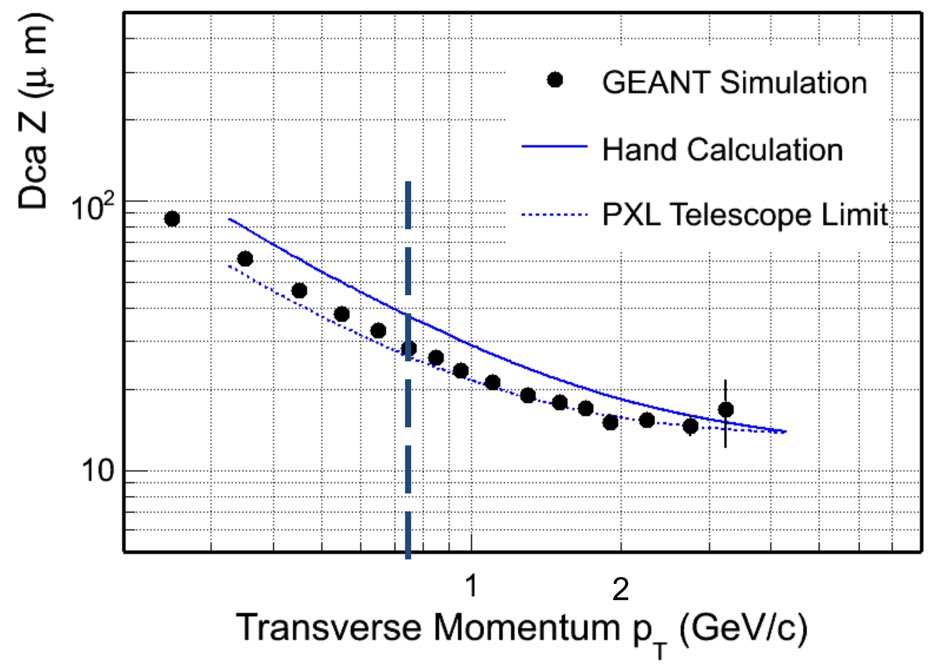


# DCA resolution performance

STAR HFT



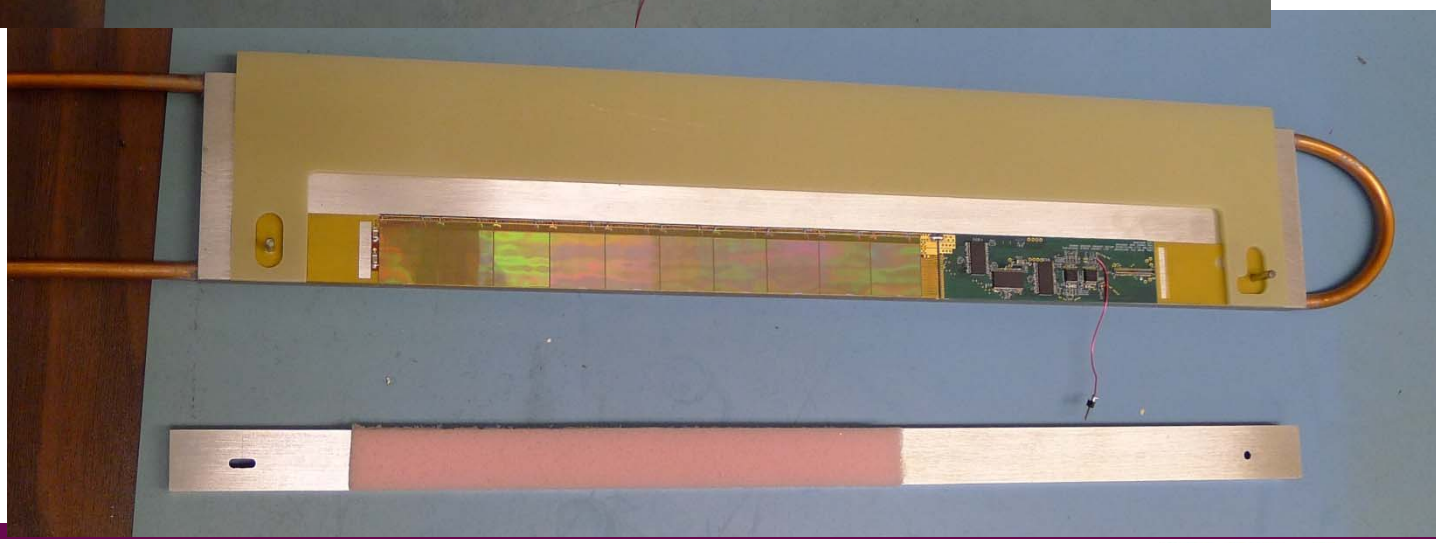




**GEANT:** Realistic detector geometry + Standard STAR tracking including the pixel pileup hits at RHIC-II luminosity

**Hand Calculation:** Multiple Coulomb Scattering + Detector hit resolution

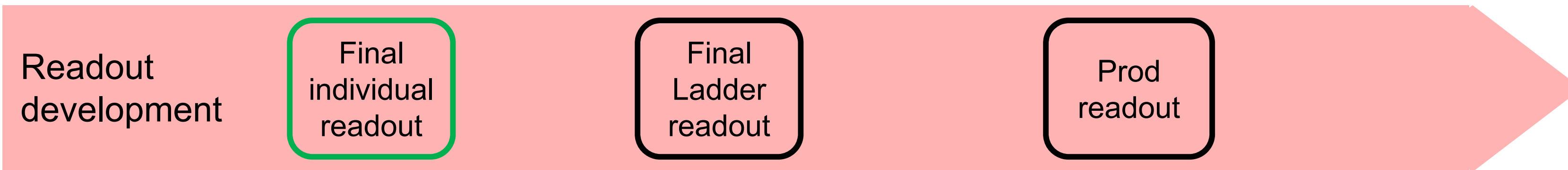
**PXL telescope limit:** Two PIXEL layers only, hit resolution only

2012/8/29 Yifei Zhang / USTC



# Read-out Electronics

STAR HFT



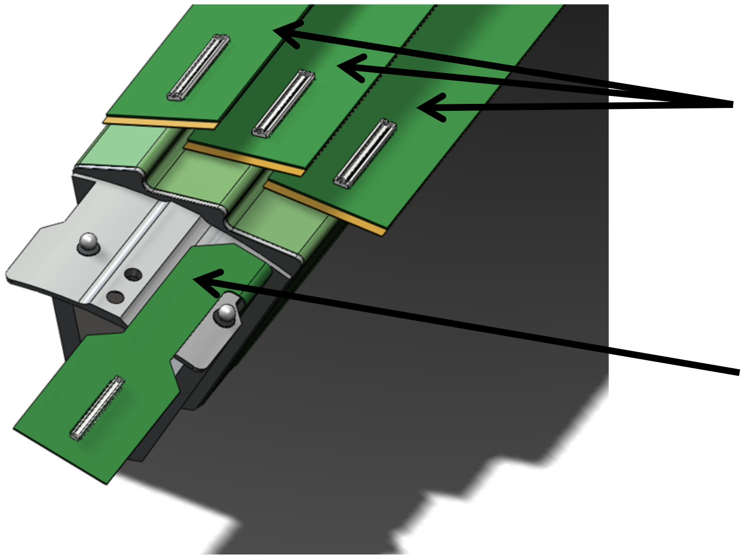

- The Xilinx Virtex-6 based RDO system motherboard has completed testing and is performing as designed.
- This board + prototype MTB were used for RDO for the Ultimate 1 prototype ladder testing.
- Based on this testing, the current RDO motherboards are the production prototype. We have placed the order for the 10 motherboards to be used in the engineering run.
- The RDO system is ahead of schedule.

# Cable Structure



Preliminary Design: Hybrid Copper / Aluminum conductor flex cable


There are two cable regions joined by wire bonds



Outer ladders have a simple rectangular driver region PCB.

Inner ladders have a complex driver region PCB that incorporates a kapton flex region to allow the ladder interface connector to be routed to the top of the sector.

# Alternate Technologies Considered

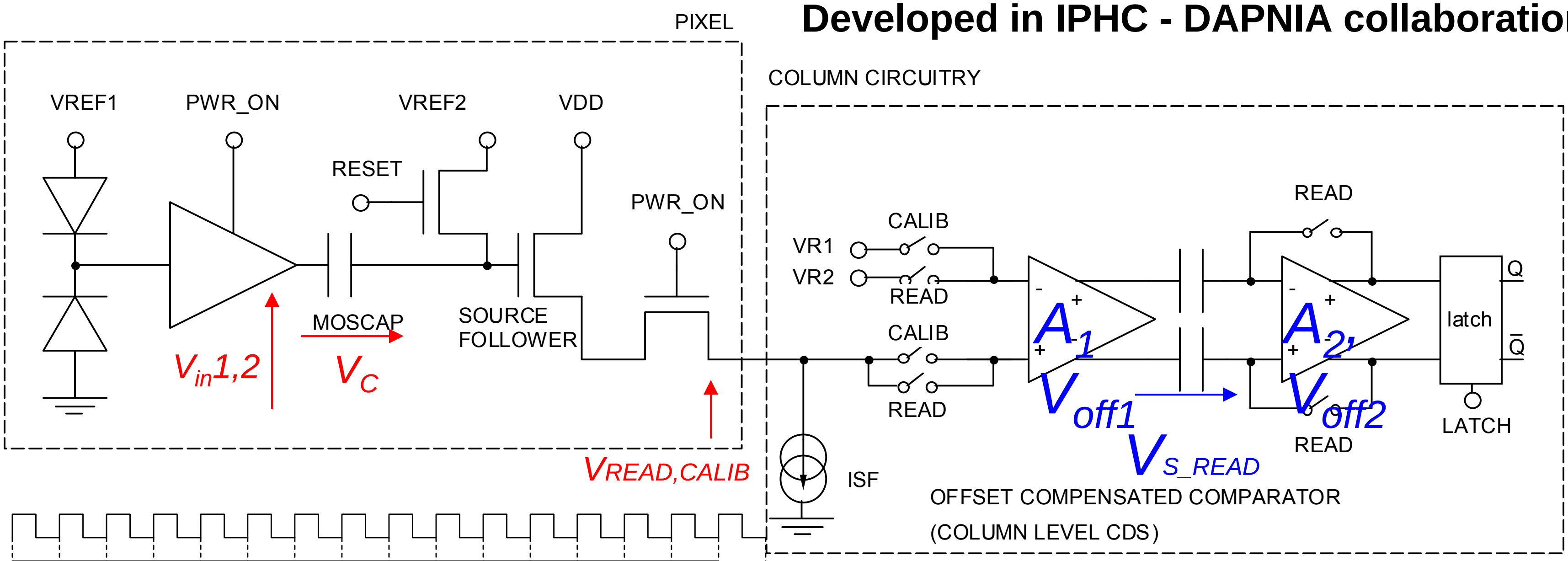


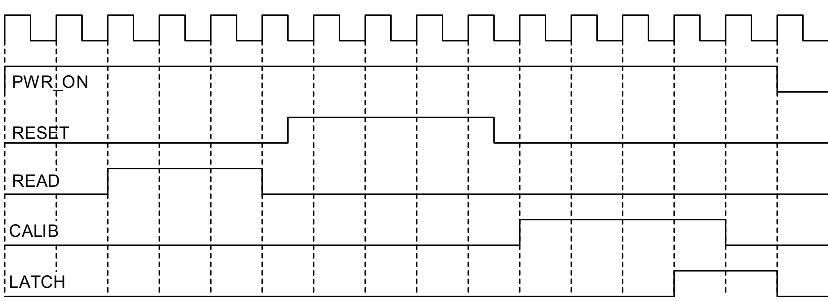
- Hybrid
  - $X_0$ large (1.2%)
  - Pixel Size large (50 $\mu$m x 450 $\mu$m)
  - Specialized manufacturing - not readily available
- CCDs
  - Limited radiation tolerance
  - Slow frame rate, pileup issues
  - Specialized manufacturing
- DEPFET
  - Specialized manufacturing
  - very aggressive unproven technology

MAPS sensors are the technology selected

# Fast, column-parallel architecture

## Developed in IPHC - DAPNIA collaboration




**CDS at column level (reduces Fixed Pattern Noise below temporal noise)**

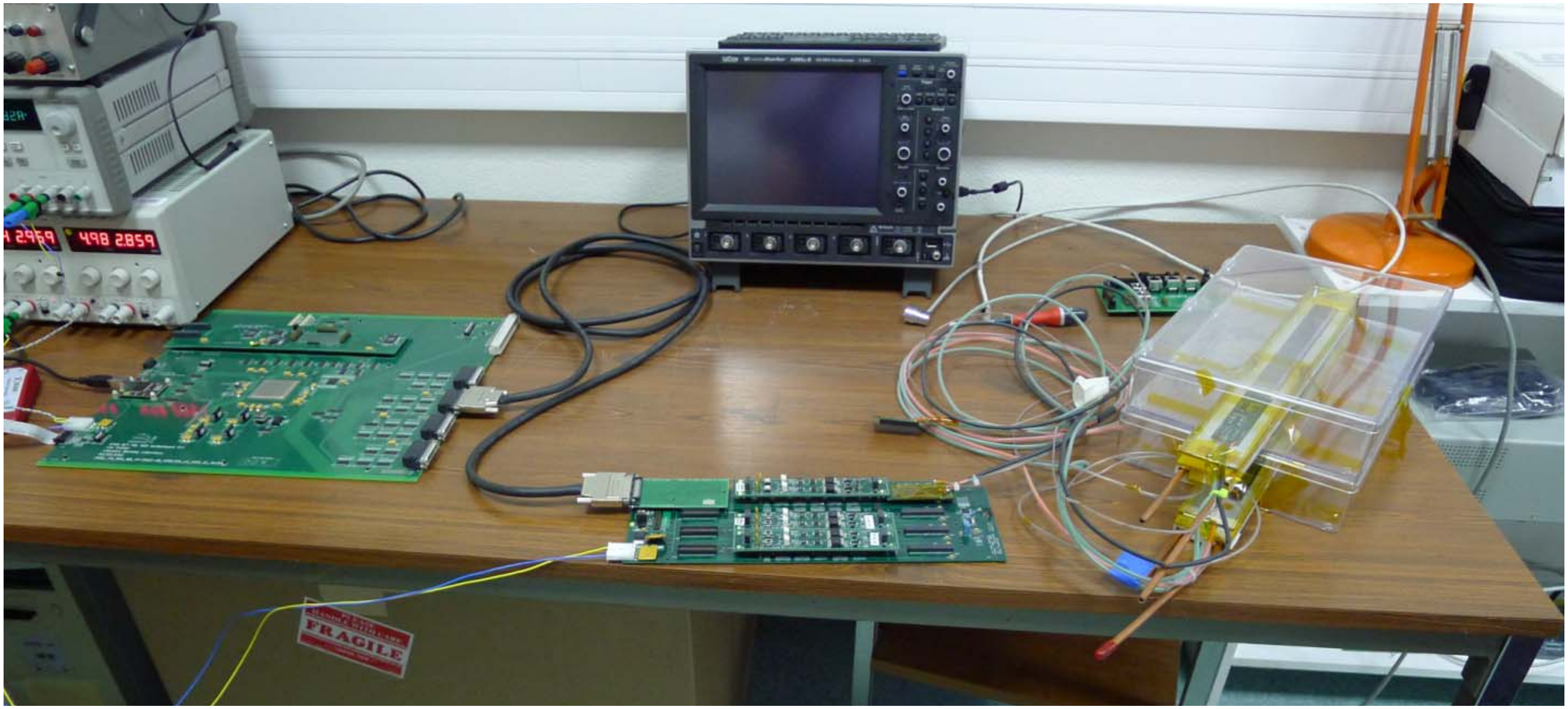
$$V_{CALIB} = V_{ref\,2} + V_{sf}\,,\quad V_C = V_{ref\,2} - V_{in1}$$

$$\begin{aligned} V_{READ} &= V_{in2} + V_C + V_{sf} = \\ &= V_{in2} + V_{sf} + \left(V_{ref\,2} - V_{in1}\right) \\ &= V_{ref\,2} + V_{sf} + \left(V_{in2} - V_{in1}\right) \end{aligned}$$

$$V_{S\_READ} = \frac{A_2}{1 + A_2} V_{off\,2} - \left(-A_1\left(V_{READ} - V_{R2} - V_{off\,1}\right)\right)$$

$$V_{out} = -A_2\left(-A_1\left(V_{CALIB} - V_{R1} - V_{off\,1}\right) - V_{off\,2} + V_{S\_READ}\right)$$

$$V_{out} = A_2 A_1\left(\left(V_{CALIB} - V_{READ}\right) - \left(V_{R2} - V_{R1}\right)\right)$$


FRAGILE

# PXL RDO Architecture (1 sector)

STAR HFT