Fully-Integrated Power Management with Switched-Capacitor DC-DC Converters

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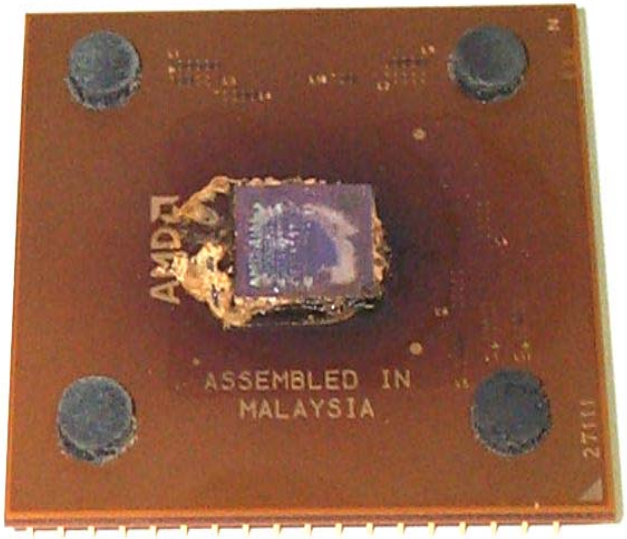
Evolution of Chip Design

- Initially driven by number of transistors/chip
- More recently, driven by the performance (freq.)
- Today, power becomes an important part of the key drivers



from http://vintagecomputerbits.com

from http://www.cobolhacker.com

ITRS Roadmap 2009

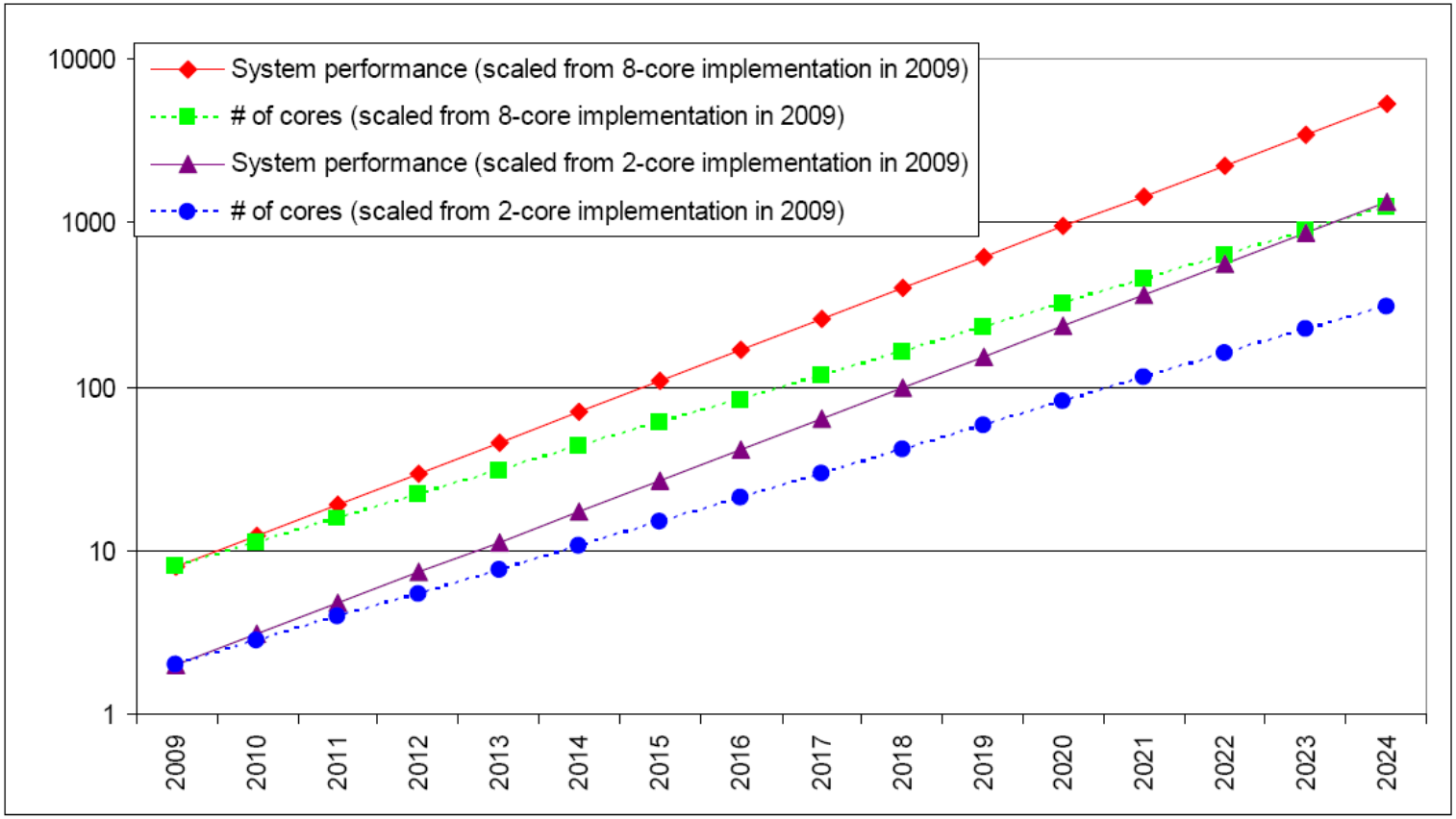
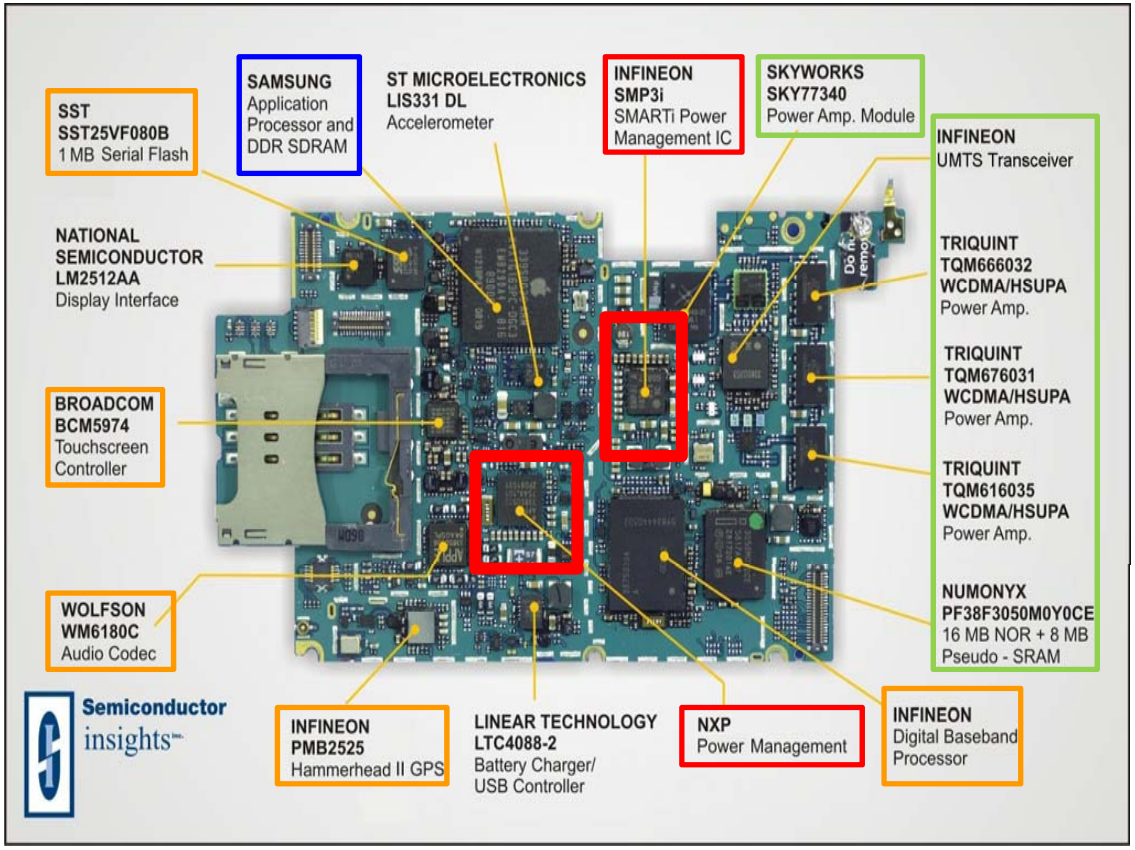


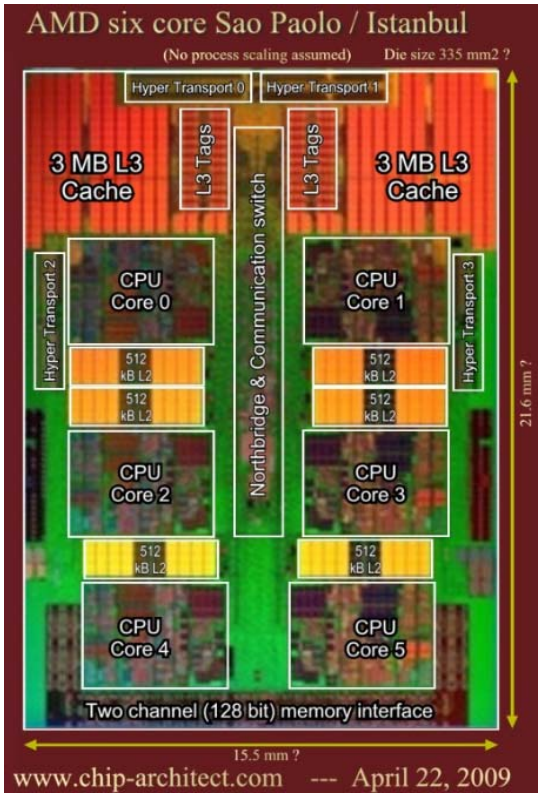
Figure SYSD2 SOC Networking Driver MC/AE Platform Performance

With constant die area:

- **Core frequency increases by 1.05× / year**
- **On-demand accelerator engine frequency increases by 1.05× / year**
- **Number of cores increases by 1.4× / year**

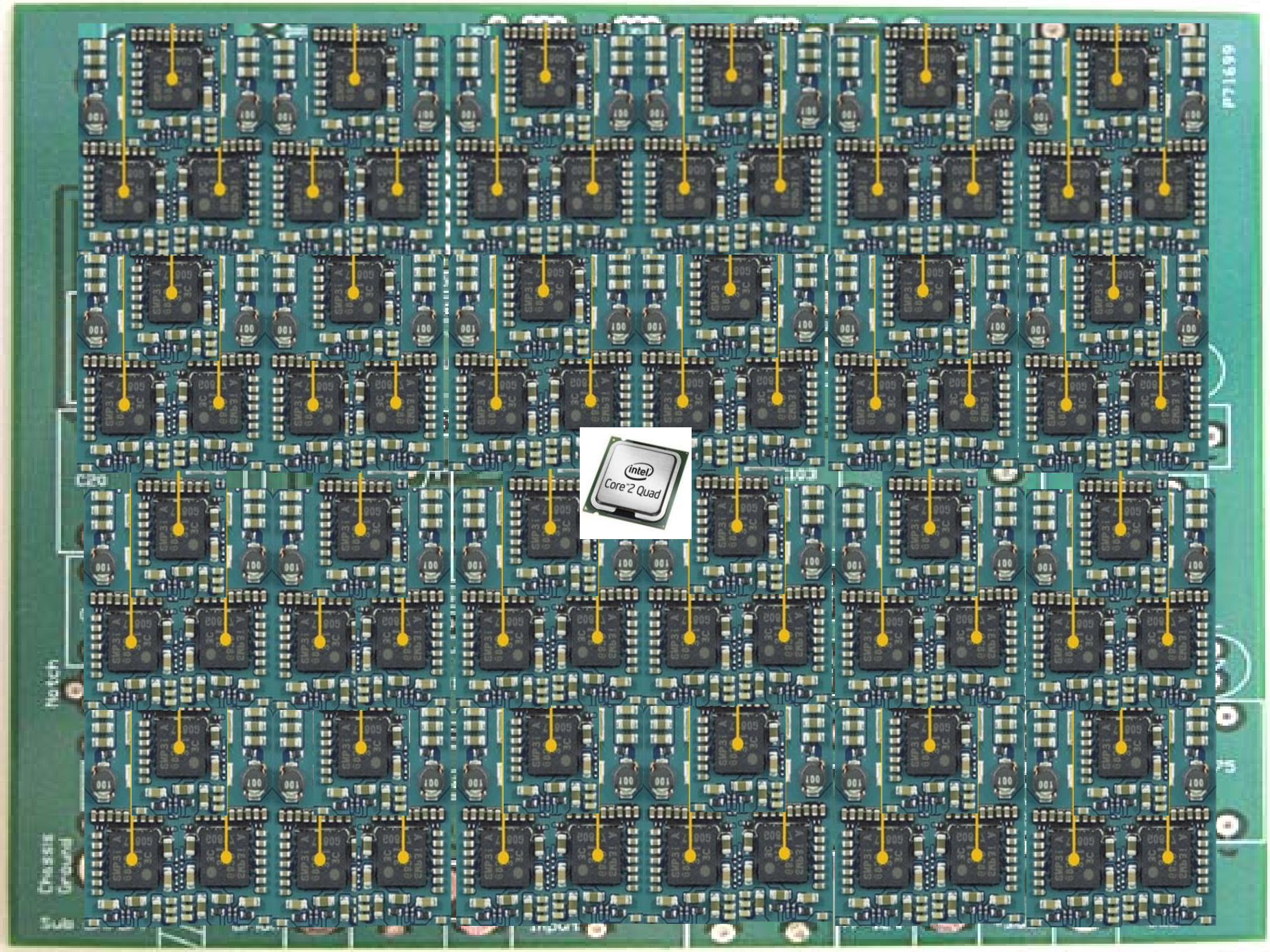
Integration Challenges



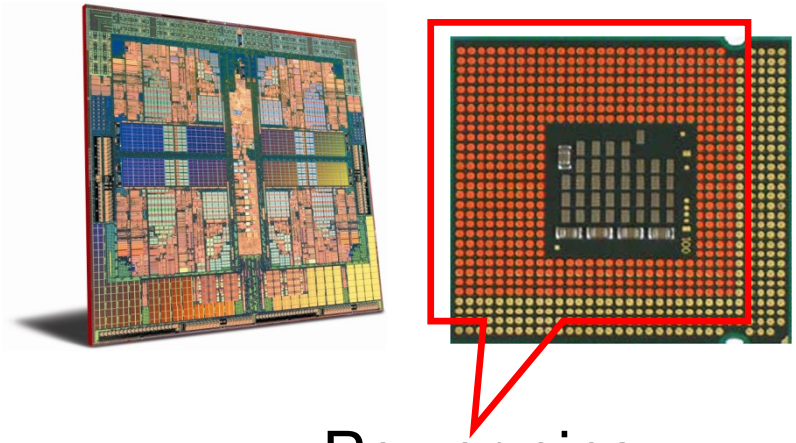


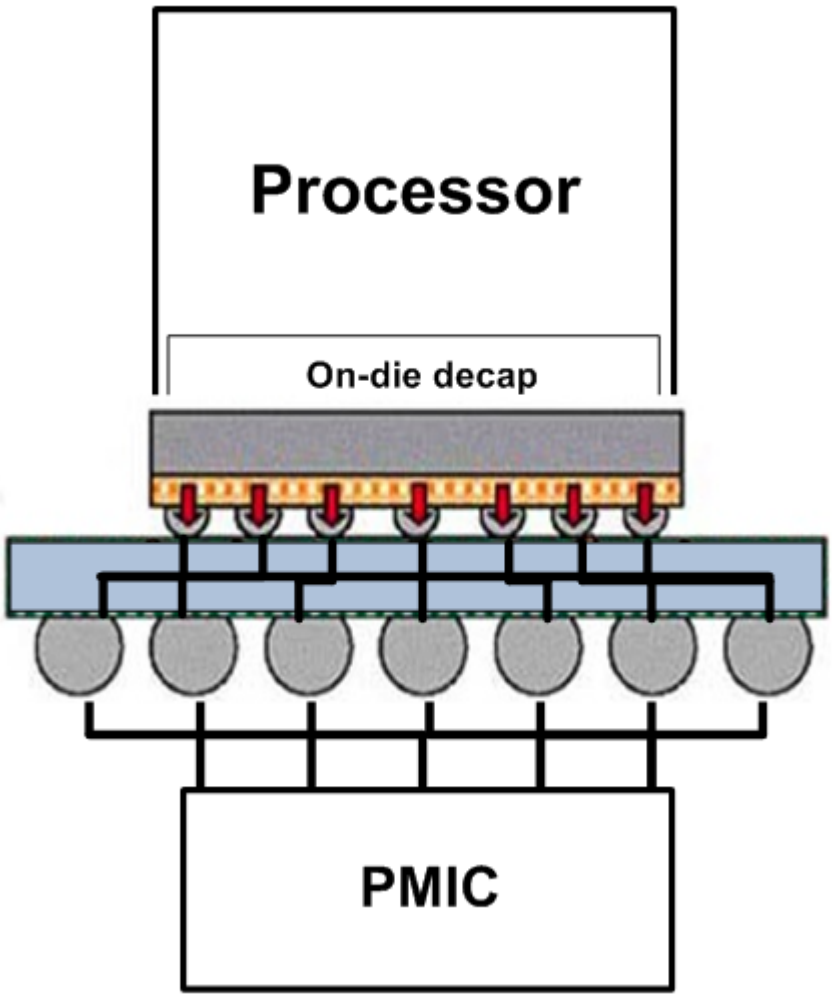
- **Integration has a benefit in energy efficiency**
  - Save IO power, board area

- **Requirement?**
  - Need different voltage supply for different blocks/IPs and different modes of operations (DVS).


intel
Core 2 Quad
Notch
Chassis ground

Limited Resources !



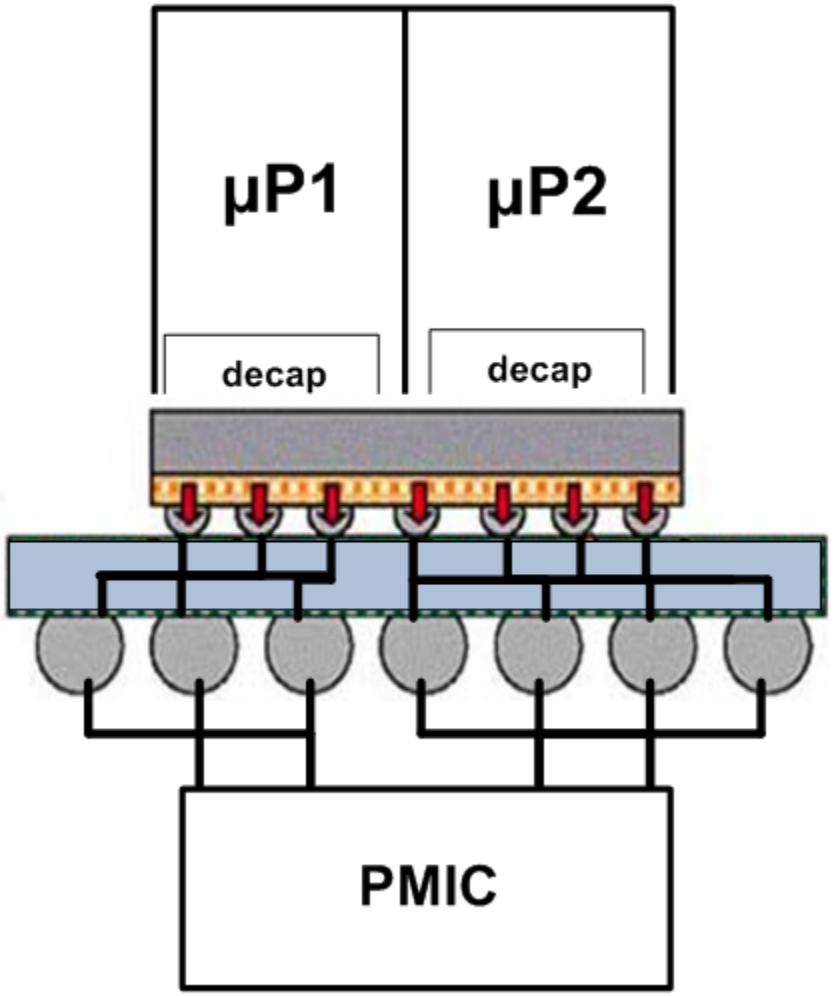


- **But the resources (pins and decap) are limited**

Multiple Off-chip Supplies: Not Appealing

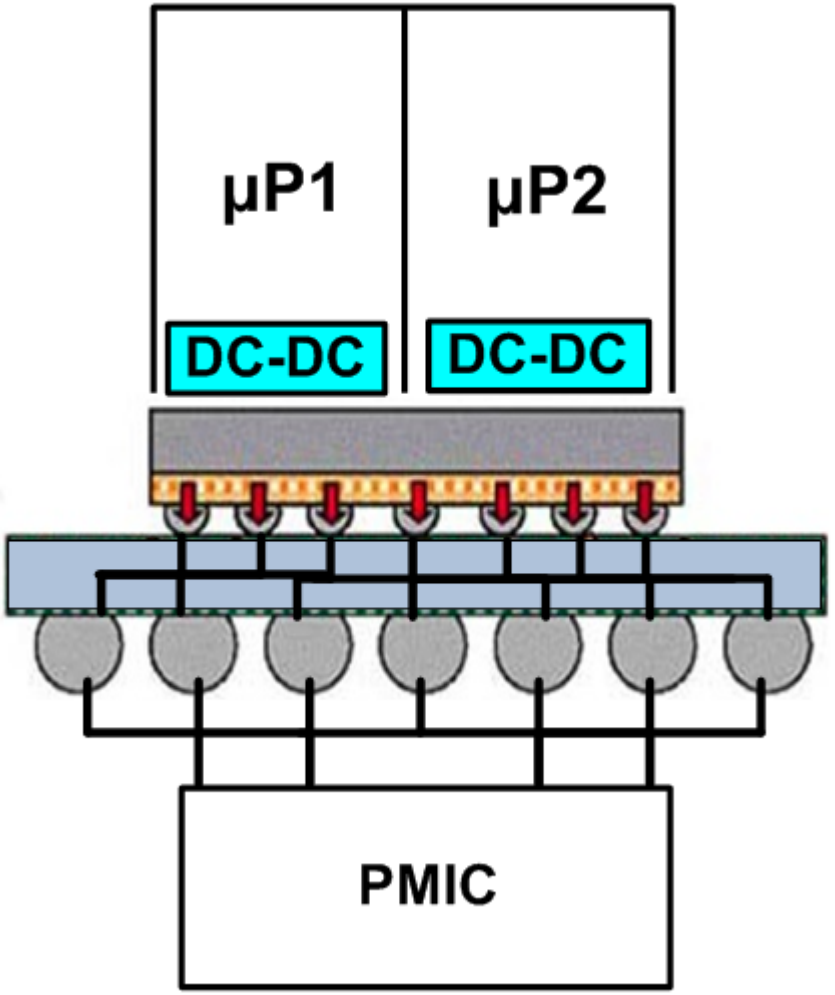
- Split power plane leads to supply impedance degradation
- Compensating by de-cap is area-consuming → costly solution

→ Just supplying power from off-chip is not appealing



Fully Integrated DC-DC Converters

- **One global supply onto die**
  - Local power generated by fully integrated DC-DC converters
- **Don't lose anything from package side**



→ How to make integrated DC-DC conversion efficient?

Outline

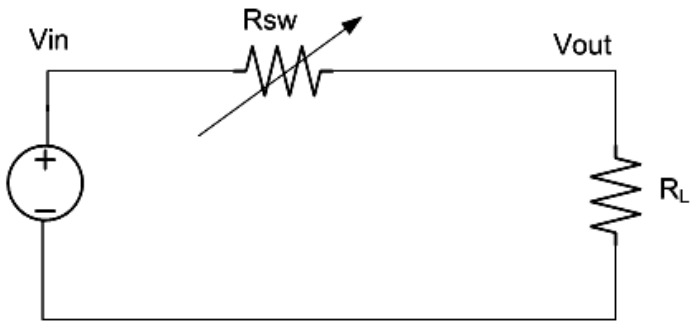
- Motivation

- Integrated converter efficiency
  - Choice of energy storage element
    - Why switched-capacitor
  - Efficiency analysis

- Switched-capacitor converter design and prototype

DC-DC Converter: Linear vs. Switching

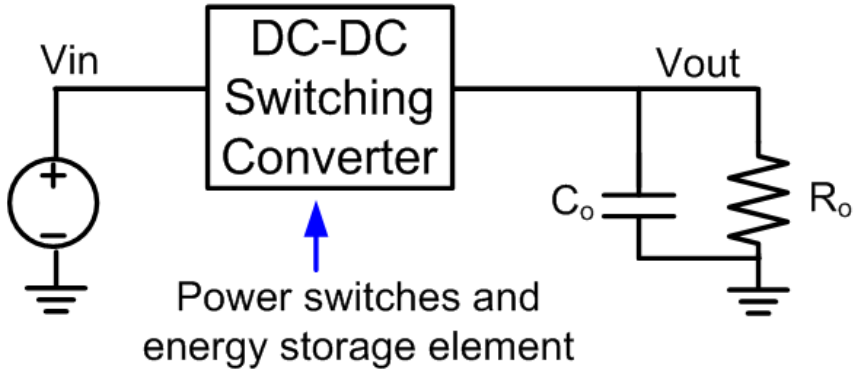
Linear Regulator



$$\eta = \frac{V_{out}}{V_{in}}$$

- Fundamental limit on efficiency

Switching Regulator

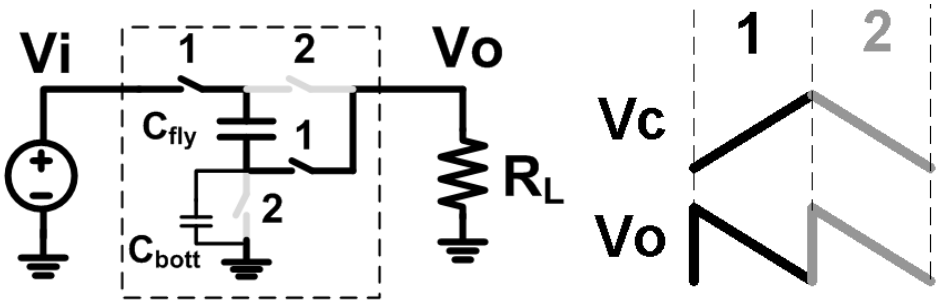


Inductor or Capacitor?

- Efficiency is ideally independent of conversion ratio.
- Theoretically, can reach up to 100% efficiency

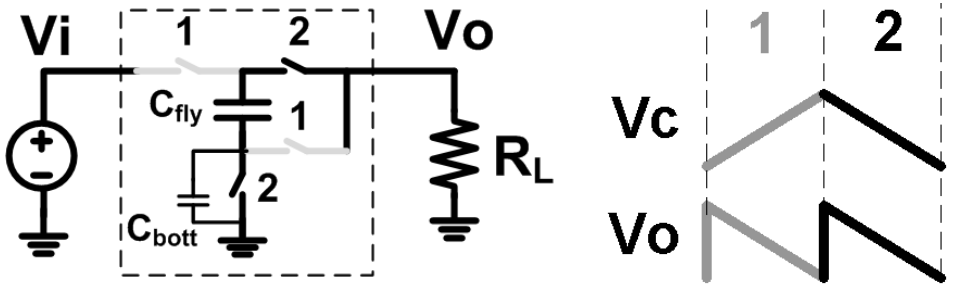
SC – Operation of 2-to-1 Conversion

Phase 1



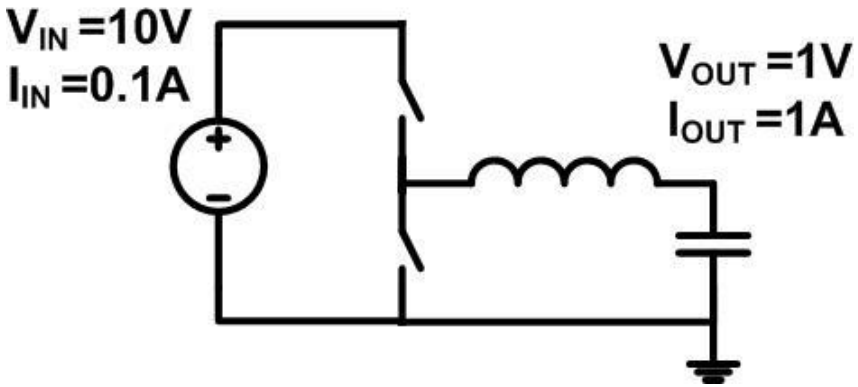
- Two-phase operation
  - Phase 1: charge capacitor

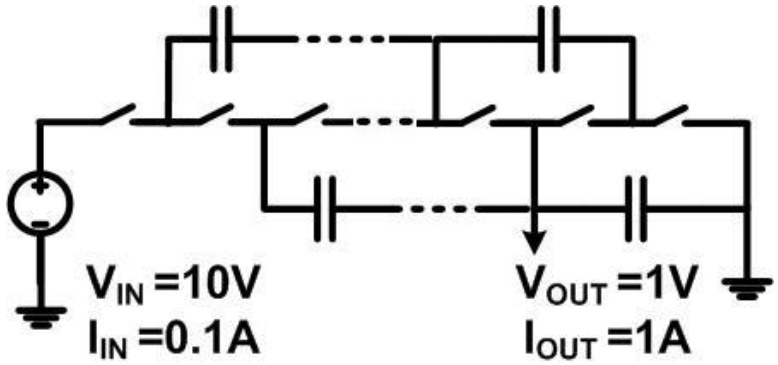
Phase 2



- Phase 2: capacitor transfers charge to output

First Look at Switch Utilization





Magnetic boost/buck:

- 10-to-1 V conversion, 1A @ 1V
- S1,S2 rated for V-A product of
  - V*I = 10 V-A
- Sum up to 20 V-A

→ Require high voltage switches

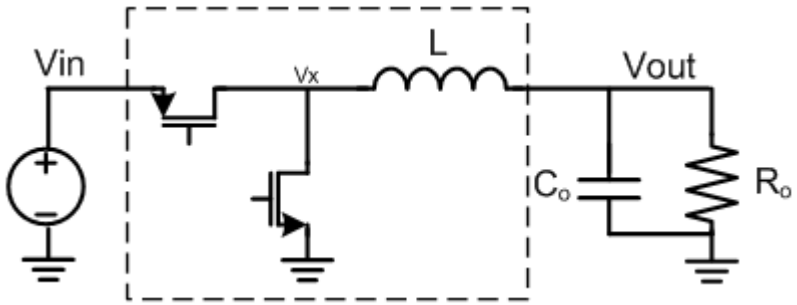
10-to-1 Ladder Switched-Cap:

- 10-to-1 V conversion, 1A@1V
- 20 switches, each blocks 1V
  - 18 switches handle 1/5 A
  - 2 switches handle 9/5 A
- V-A product sums up to 36/5 =7.2 V-A

→ Native CMOS device convenient

Energy Storage Element

Inductor



- Very popular for a wide range of off-chip applications

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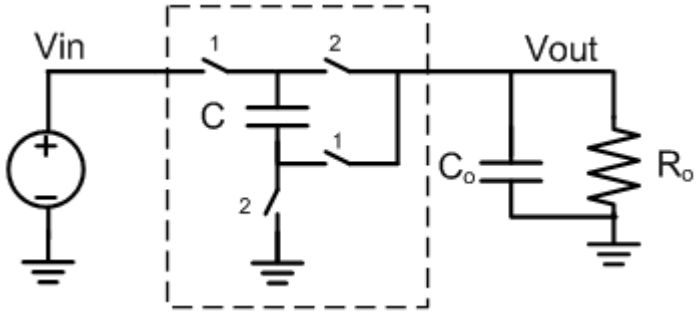
- Standard CMOS inductors have high series resistance → low efficiency

- **Technology modifications are costly**

Capacitor



- Usually considered appropriate for "low power"

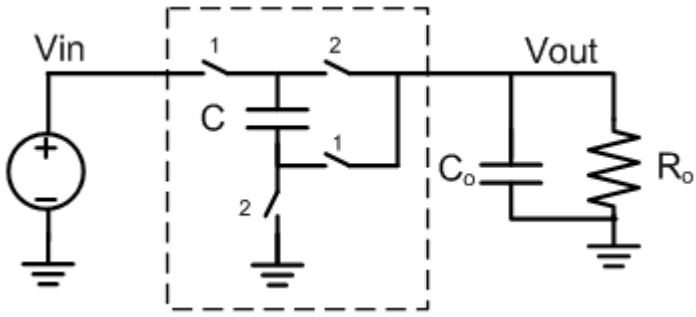
- - - - - -

- High Q, high capacitance density.

- **Highly compatible with commercial CMOS process**

Switched Capacitor Power Converters

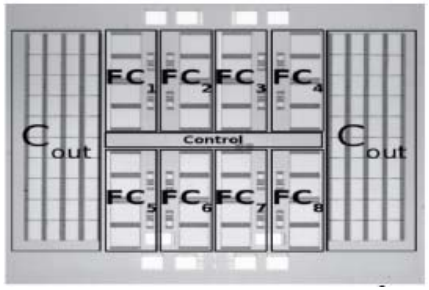
- **Only switches and capacitors**
- **Using no inductors has advantages:**
  - Simplified full integration potential
  - Works well over a wide power range
    - Single mode, can adjust clock rate
    - No minimum load
  - No inductive switching losses



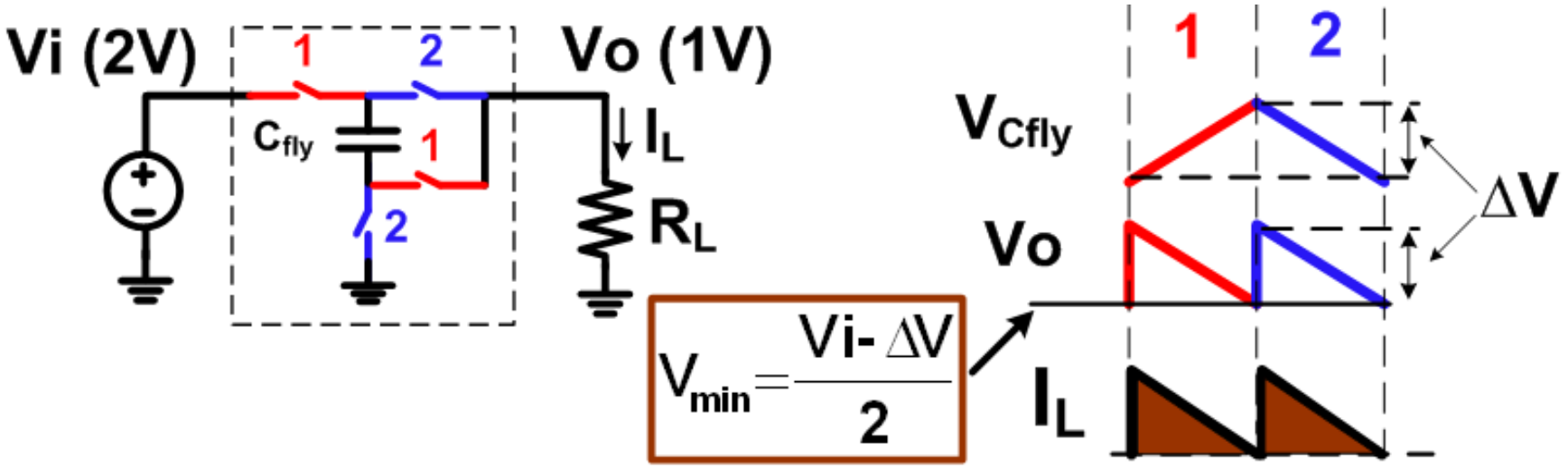
Why Not S-C ?

- Voltage rating of CMOS processes?
- Not suited for high current/power?
  - Magnetic-based ckts = higher performance?
- Ripple?
- Interconnect difficulty for many caps?
- Difficult regulation?

Previous Work

Work	[1] Breussegem, VLSI 09	[2] Somasekhar, VLSI 09
Technology	130nm Bulk	32nm Bulk
Topology	2/1 step-up	2/1 step-up
Interleaved Phases	16	32
Converter Area (mm^2)	2.25	6.678×10^{-3}
Power density @ η_{max}	2.09 mW/mm^2	1.123 W/mm^2
Efficiency (η_{max})	82%	60%
Die photo		

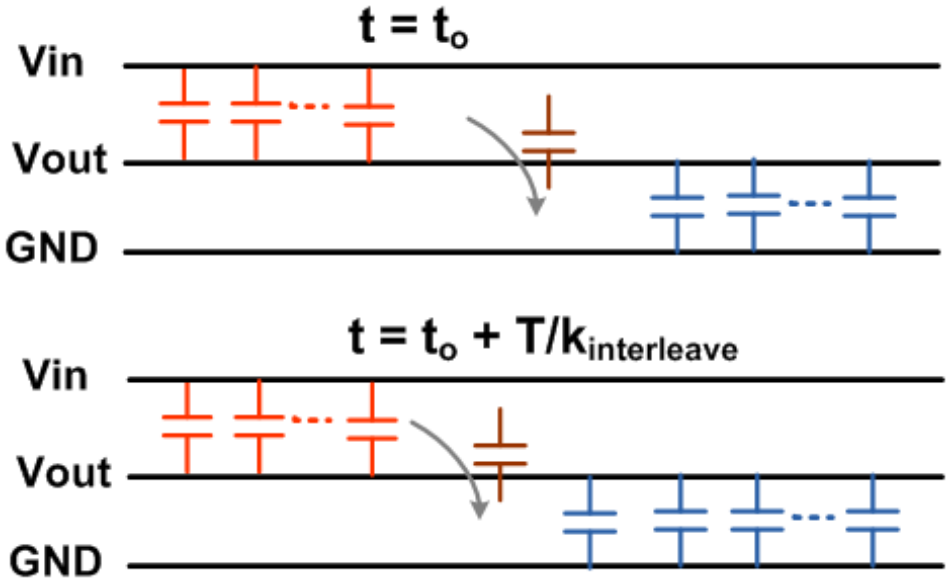
Switched Capacitor Loss

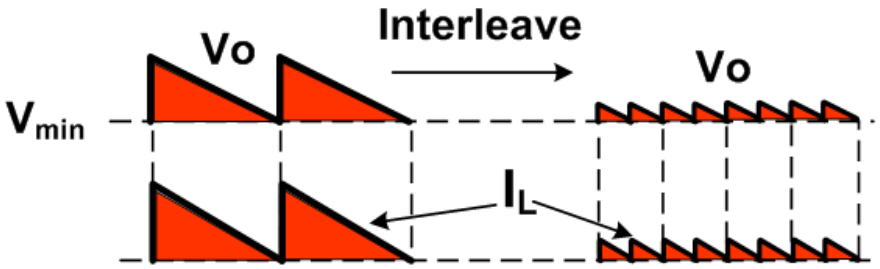


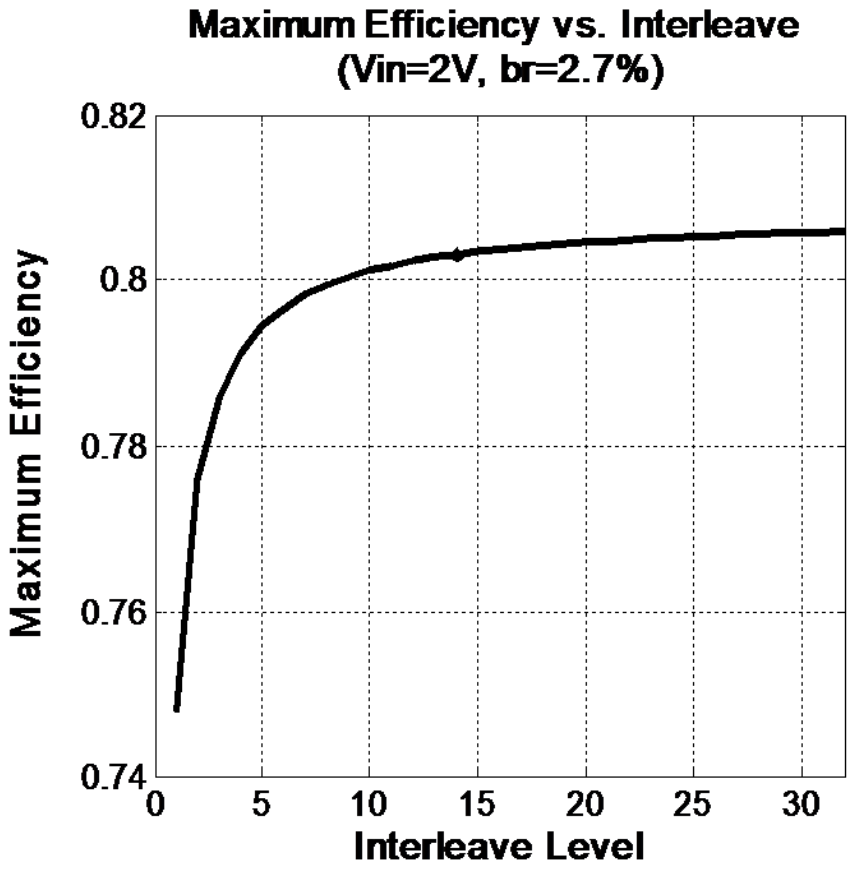
- **Converter supplies digital circuits**
  - Performance (f_{CPU}) set by V_{min}
- **Intrinsic switched-capacitor loss:**

$$P_{C_{fly}} = 2x \frac{I_L^2}{M_{conv,cap} f_{sw} C_{fly}}$$

Multi-Phase Interleaving





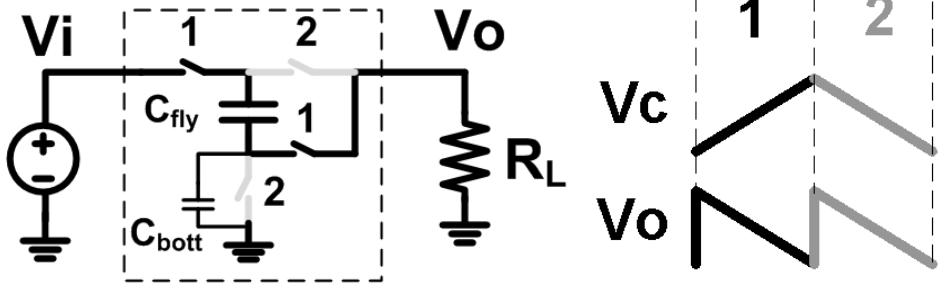


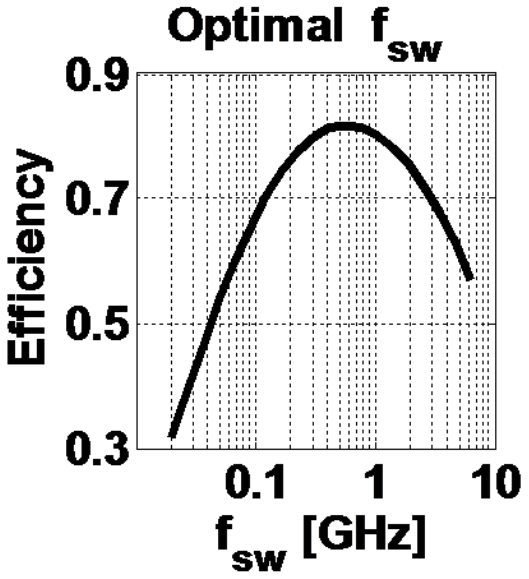
- **Good news:**
  - Interleaving can reduce ripple without changing V_{min}

$$P_{C_{fly}} = \left(1 + 1/k_{interleave}\right) \frac{I_L^2}{M_{conv,cap} f_{sw} C_{fly}}$$

Ref: D. Ma, F. Luo, *IEEE Trans. VLSI Sys.*, 2008

SC – Loss Optimization





- **4 main loss components**

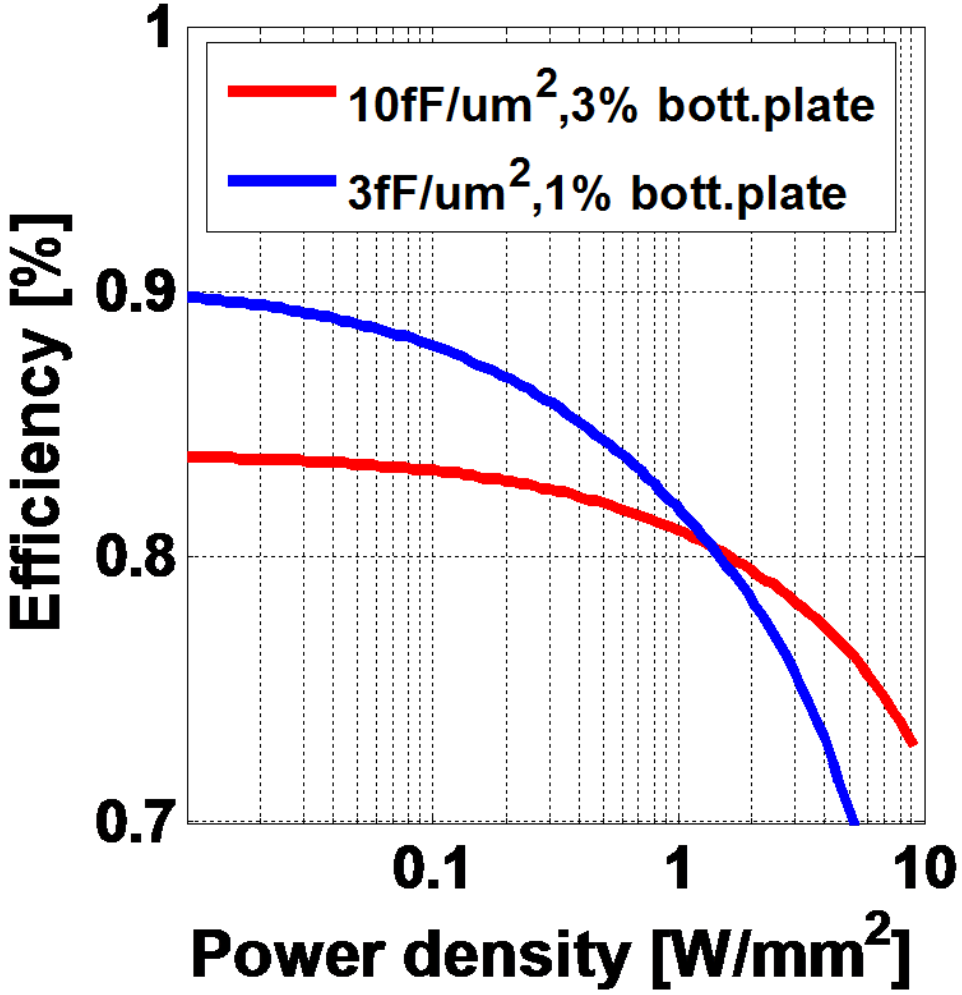
$$P_{loss} = P_{Rsw} + P_{C_{fly}} + P_{bott.cap} + P_{gate.cap}$$

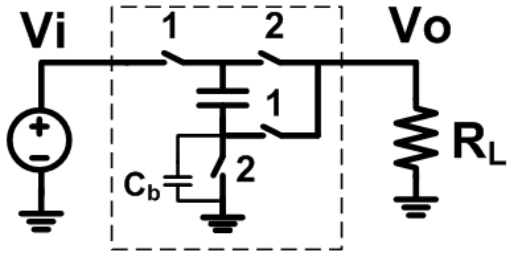
$$\alpha \; I_L^2 \frac{R_{on}}{W_{sw}} \qquad \alpha \; \frac{I_L^2}{f_{sw} C_{fly}} \qquad \alpha \; C_{bott} f_{sw} \qquad \alpha \; W_{sw} C_{gate} f_{sw}$$

Switch resist. | Switched cap | Bottom Plate | Gate loss

Series Losses (Ro) | Parasitic Losses ($R_{//}$)

Optimization for Efficiency





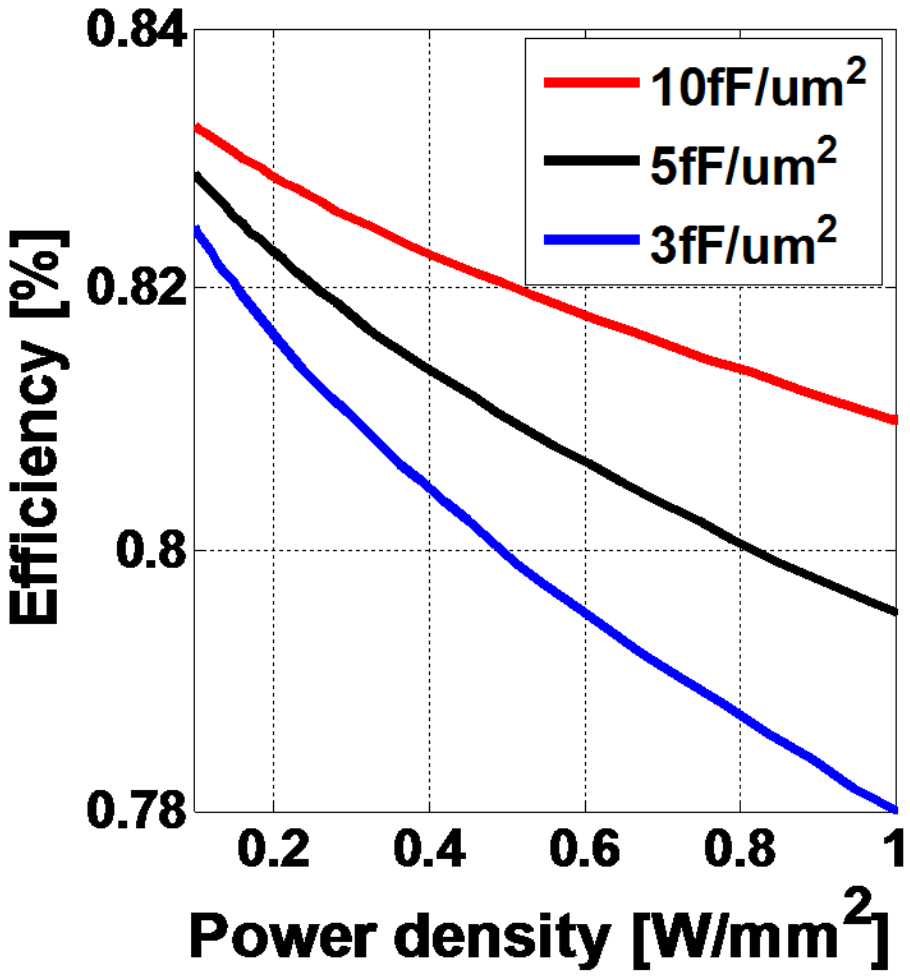
- **Efficiency trades off with power density**
- **Low power density:**
  - Bottom plate critical
- **High power density:**
  - Flying cap critical

$$\frac{P_{loss}}{P_{Load}} \approx \sqrt{M_{conv} k_{bott}} + \sqrt{\frac{1}{\sqrt{M_{conv} k_{bott}}} \frac{V_{sw}^2 R_{on} C_{sw}}{V_o^2 R_L C_{fly}}}$$

Achievable Performance

- **Looks promising**
  - Especially in mobile applications
  - 1W/mm^2 converter fits in decap area
- **Only looked at 2:1 converter so far**
  - Need to support multiple output voltage levels

Eff. vs. Cap Density (k_{bott} = 3%)



Outline

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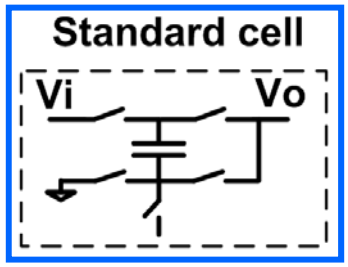
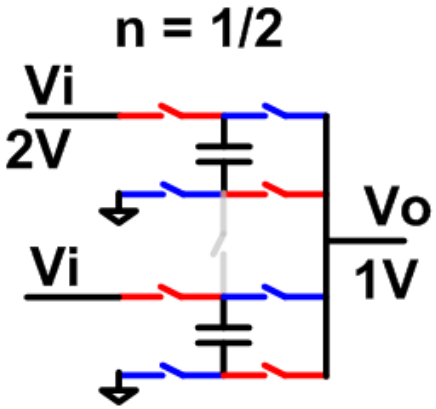
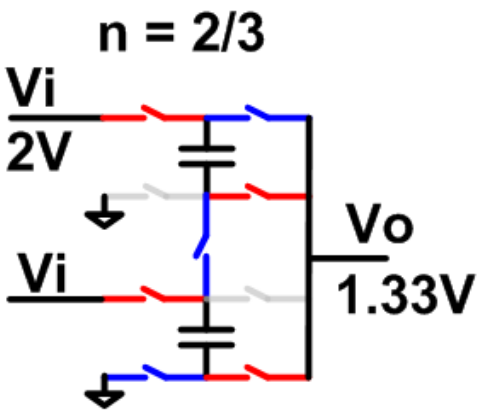
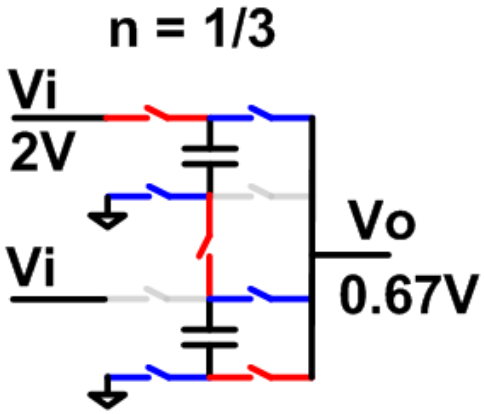
- Switched-capacitor converter design and prototype

Multiple Conversion Ratios

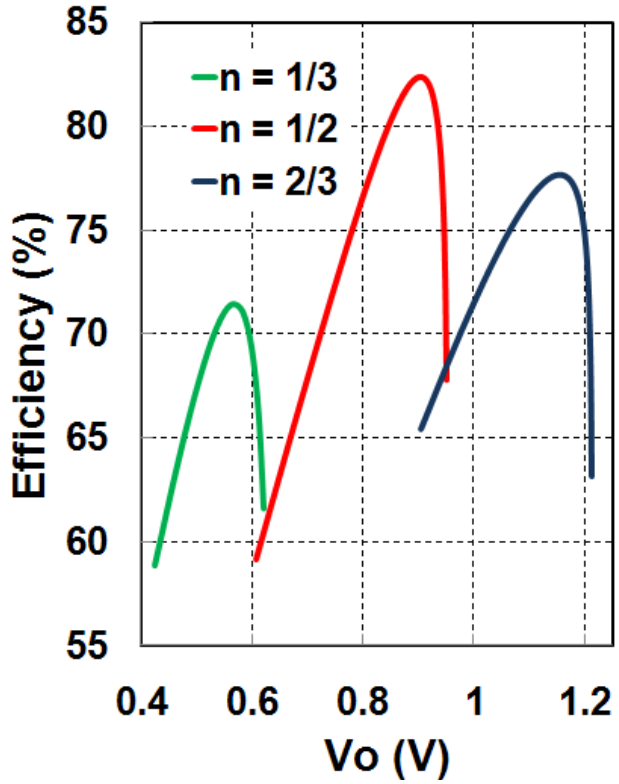






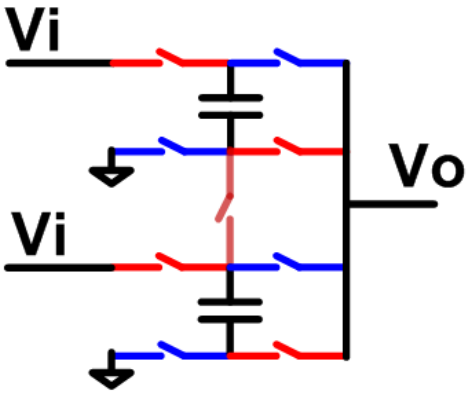


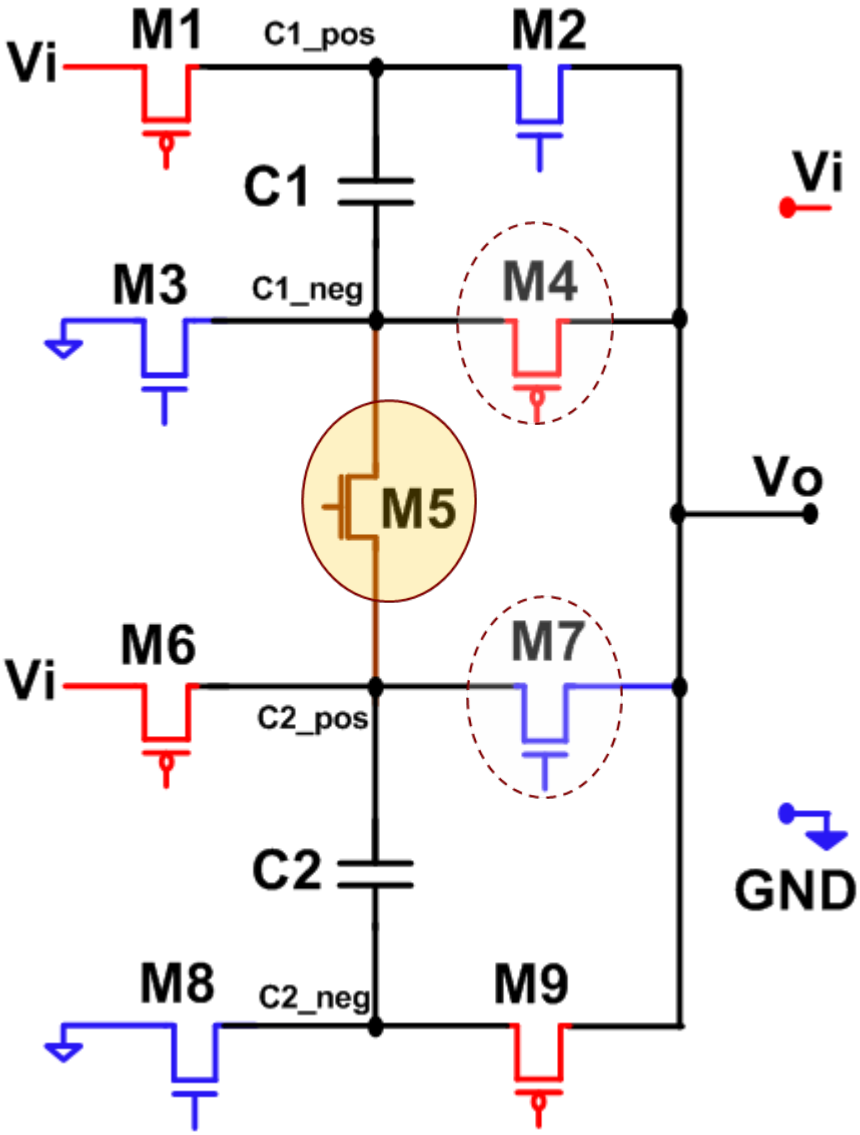
- **Standard cell design supports multiple conversion ratios**
- **Fine output voltages achieved by controlling f_{sw} (or W_{sw})**
  - Equivalent to linearly regulating down from peak efficiency
- **How to drive the switches?**



Ref: D. Maksimovic and S. Dhar, *IEEE PESC, 1999*

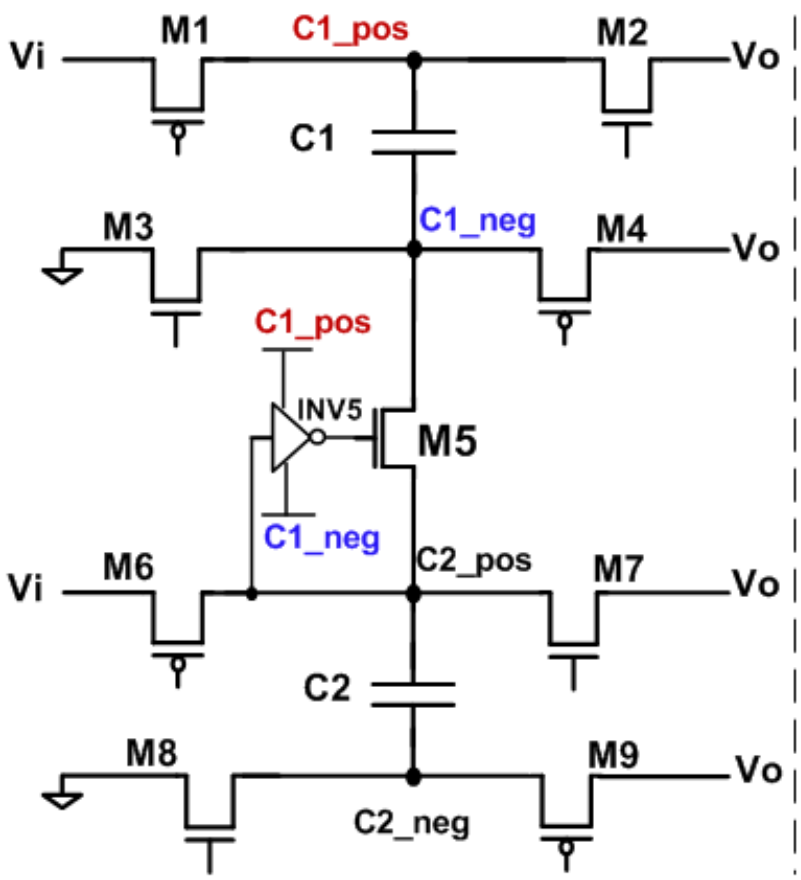
Switch Drivers

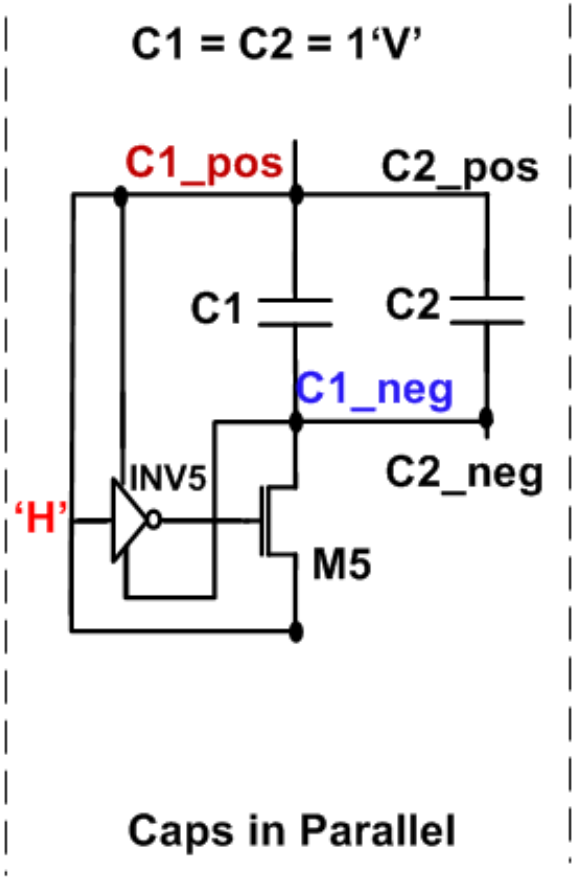


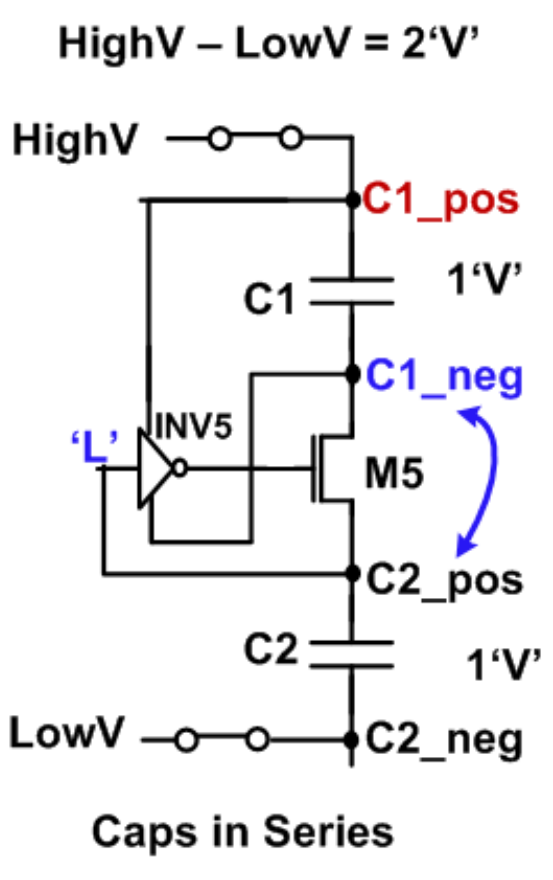


- **Most switches easy to drive**
  - 2 voltage domains:
    - (Vi – Vo)
    - (Vo – GND)
- **M4, M5, and M7 challenging**
  - Experience voltages between the two domains

Switch Driver – M5

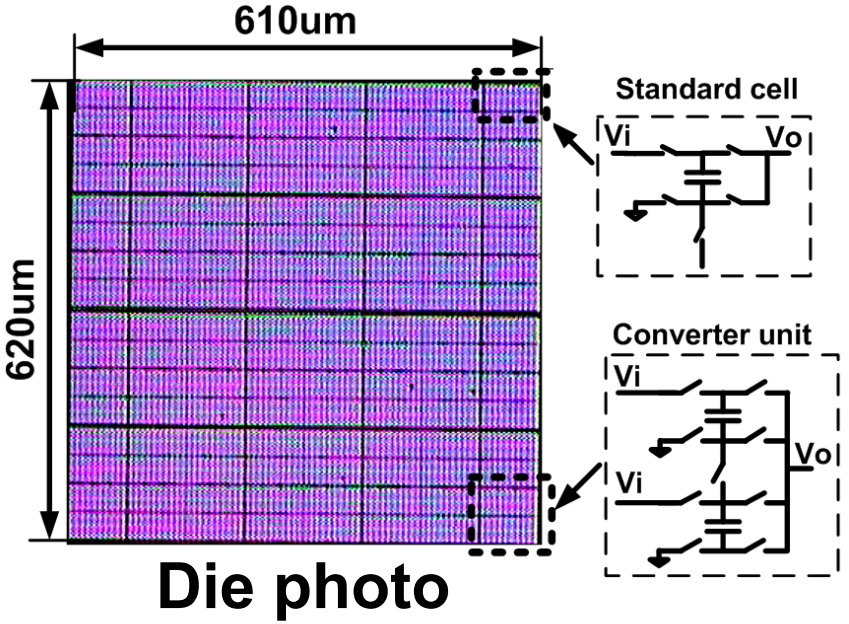






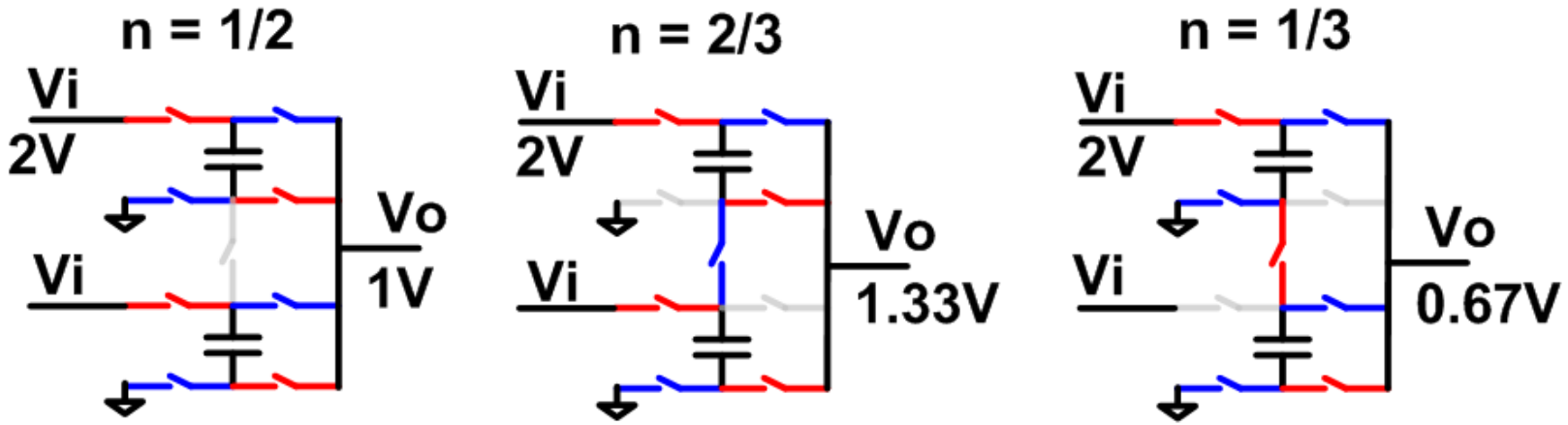
- **"Flying" inverter INV5 powered off of C1**
  - Controlled by top-plate of C2
- **Automatically synchronized by operation of other switches**

SC Converter Prototype

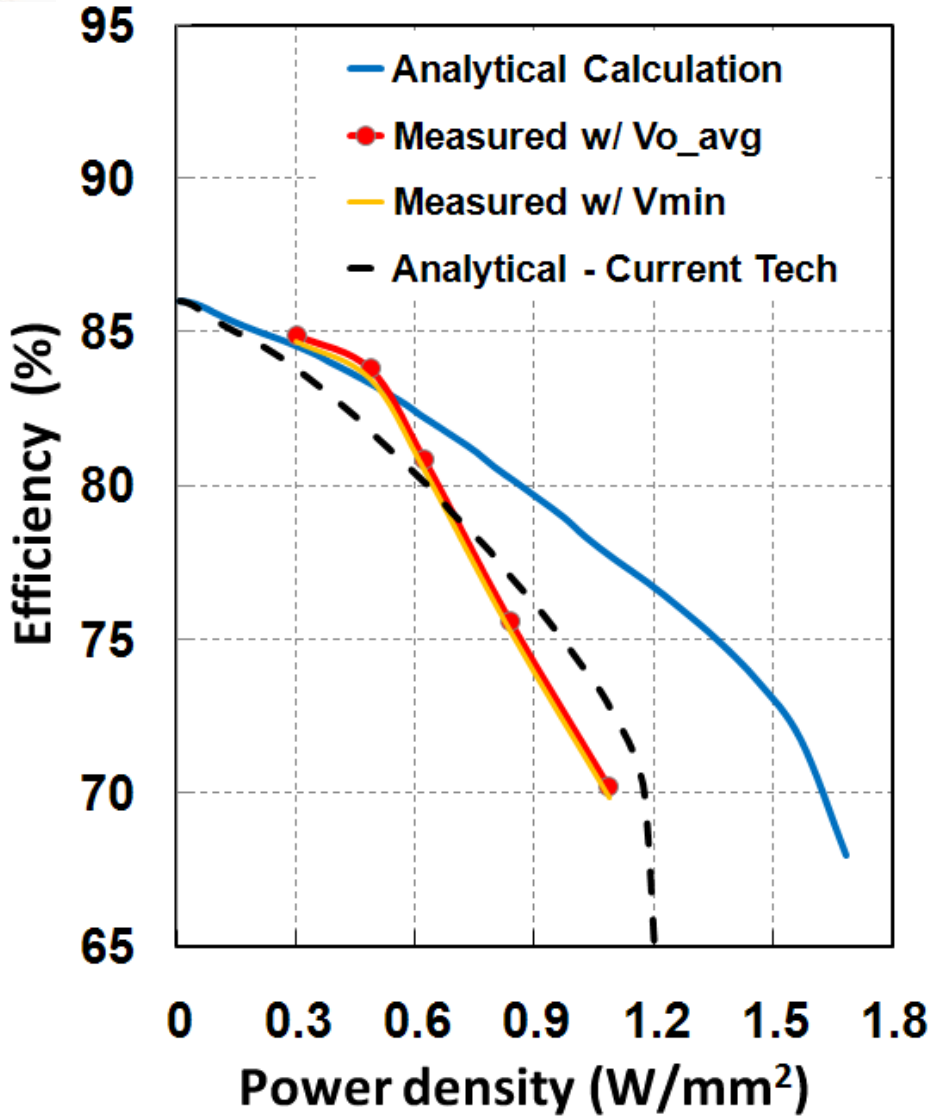


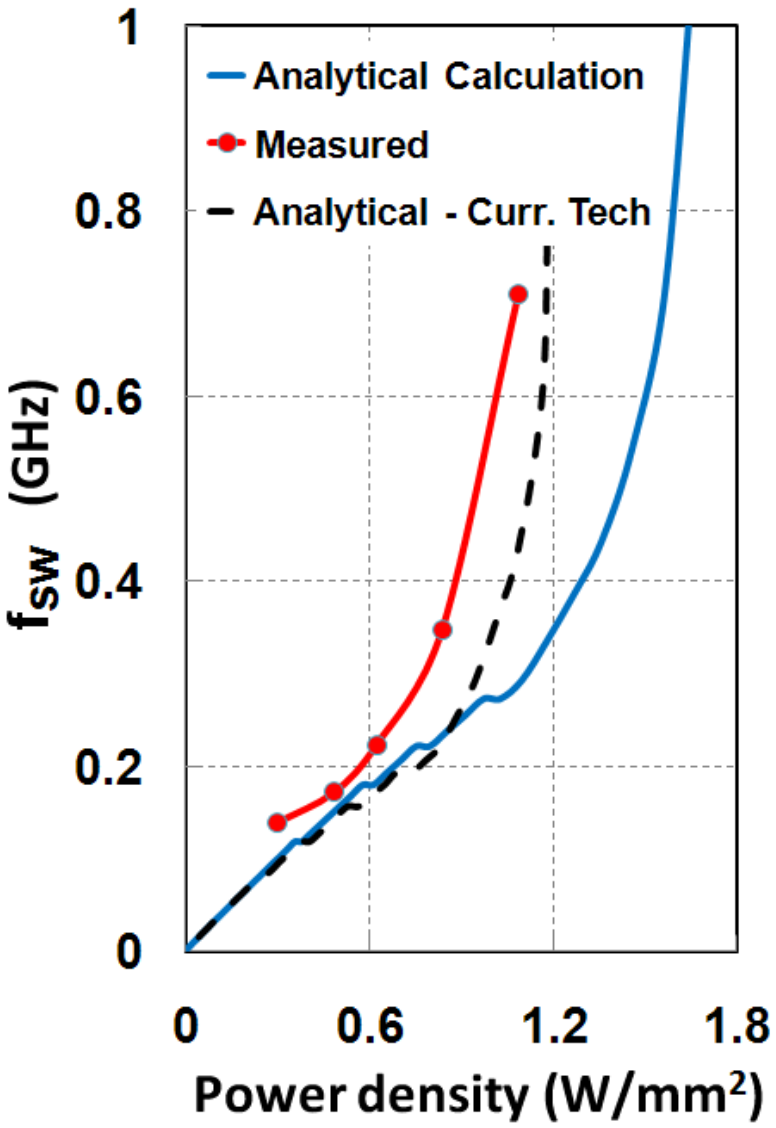
Die photo

- Implemented in 32nm SOI test-chip
- Flying cap: MOS, 32-way interleaved
- Supports 0.6V ~ 1.2V from 2V input



Measured Eff. vs. P-density

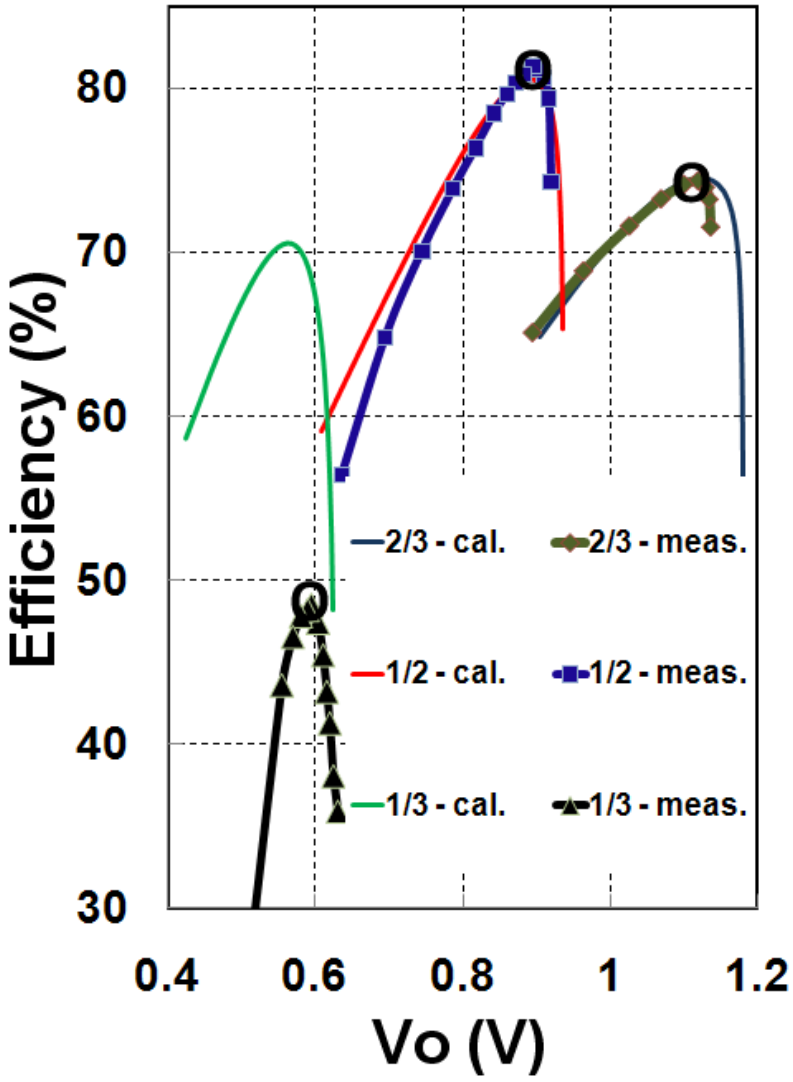




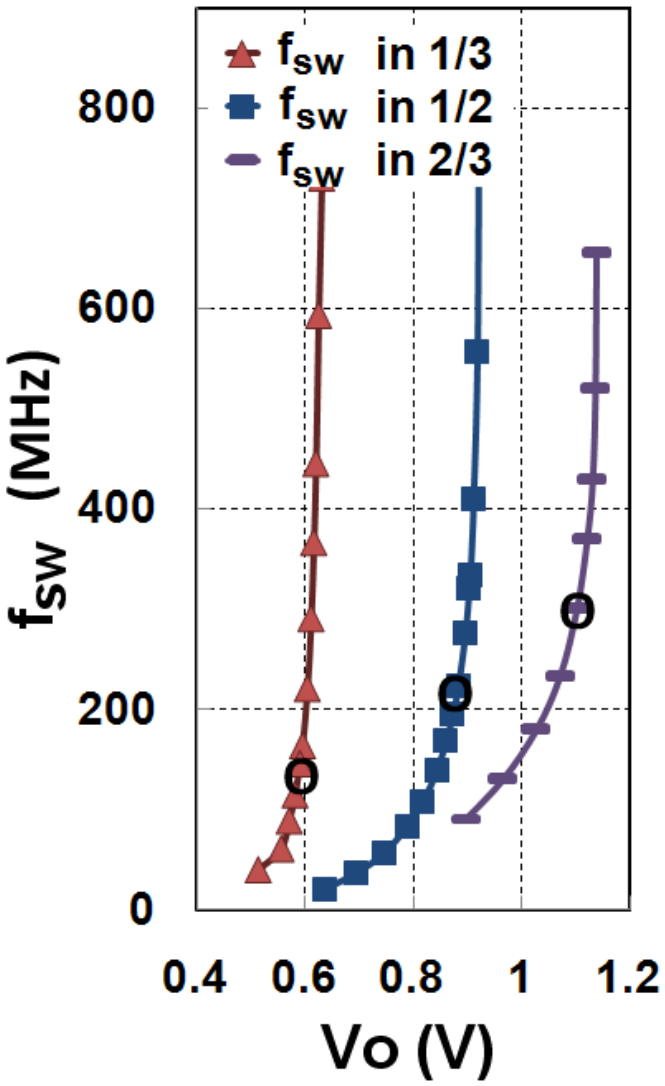
- Measured in 1/2 mode (Vi = 2V, Vo ≈ 0.88V)
- Results promising: 82% efficiency @ 0.55 W/mm²

Measured Eff. vs. Topologies

Efficiency vs. Vo



f_{sw} vs. Vo



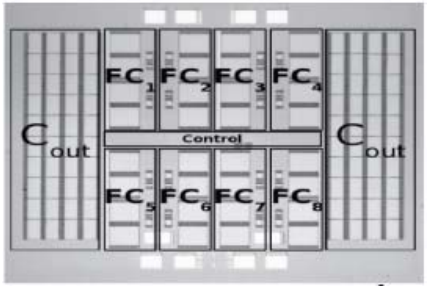
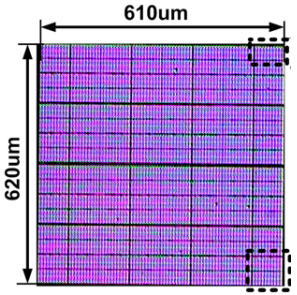
Settings:

Vi = 2V

$R_L \approx 4\Omega$ at

Vo = 0.8V

Previous Work

Work	[1] Breussegem, VLSI 09	[2] Somasekhar, VLSI 09	This work
Technology	130nm Bulk	32nm Bulk	32nm SOI
Topology	2/1 step-up	2/1 step-up	step-down 1/2, 2/3, 1/3
Interleaved Phases	16	32	32
Converter Area (mm^2)	2.25	6.678×10^{-3}	0.36
Power density @ η_{max}	2.09 mW/mm^2	1.123 W/mm^2	0.55 W/mm^2
Efficiency (η_{max})	82%	60%	82%
Die photo			

Conclusions

- **Clear need for fully-integrated DC-DC converters**
  - Switched–capacitor converters a promising option
- **Design optimization enables both high power density and high efficiency**
  - In 2:1: 82% efficiency at 0.55W/mm^2
- **Reconfiguration supports wide output voltage range**
  - >70% efficiency for Vo from ~0.75V to 1.15V with Vin = 2V

Why Not S-C ?

- √ Voltage rating of CMOS processes?
- √ Not suited for high current/power?
  - Magnetic-based ckts = higher performance?
- √ Ripple?
- √ Interconnect difficulty for many caps?
- √ Difficult regulation?